APPLIED PHYSICS LETTERS **96**, 083304 (2010)

Thickness-dependent *in situ* studies of trap states in pentacene thin film transistors

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(Received 17 November 2009; accepted 15 January 2010; published online 24 February 2010)

In this letter, we present *in situ* transport measurements of pentacene thin film transistors, particularly investigations of the evolution of mobility, threshold voltage, and hysteresis during the deposition of pentacene with submonolayer precision. We observe both, a strong positive shift of the threshold voltage and a reduction in the hysteresis up to a nominal pentacene film thickness of four monolayers. In addition to previously published volume electron trap states that account for the threshold voltage shift, we suggest that the existence of shallow pentacene trap states located at the free pentacene surface explains the reduction of the hysteresis. © *2010 American Institute of Physics*. [doi:10.1063/1.3309685]

The conduction channel of organic thin film transistors (OTFTs)[1,2] involves only the first few organic thin film monolayers (MLs) adjacent to the dielectric. In order to understand the transport mechanism including limitations, e.g., trap states,[3,4] it is essential to investigate transistors with organic thin films that match the Debye length[5–7] of a few ML.[8–10]

In this letter, we present *in situ* measurements of pentacene bottom contact TFTs. We investigate the evolution of the extrinsic mobility, the threshold voltage and the hysteresis during pentacene deposition with sub-ML thickness resolution. We additionally propose a model with both electron volume trap states, and shallow trap states at the free pentacene surface, which have previously not been taken into account.

The TFTs are fabricated on a highly n-doped Si substrate, which serves as the back gate, with 150 nm SiO_2 on top. In order to avoid OH-groups at the interface, we spincoat a 7 nm-thick buffer layer of either cyclic olefin copolymer or polystyrene on most of the samples. A 30 nm-thick gold layer is evaporated through a shadow mask, defining our TFT channels of 25 μm channel length. Then the samples are glued in a chip carrier, bonded, and transferred together with a pentacene shadow mask on top, in the *in situ* measurement chamber with a base pressure of about 10^{-8} mbar. The pentacene shadow mask defines our channel width of 3.5 mm.

The *in situ* measurement scheme is shown in Fig. 1. A very slow pentacene evaporation rate of about 0.02 Å/s in combination with a fast voltage sweeping rate of 4 V/s guarantees that the pentacene layer thickness varies only on the order of 1 Å during one voltage sweep, which is far below the thickness of a ML of the pentacene thin film phase of 15.4 Å.[11] One measurement cycle consists of five transconductance gate-voltage sweeps from +40 to −40 V (off-to-on gate-sweeps) and back, at a constant source-drain-voltage V_{SD} of −20 V. Subsequently, a single conductance source-drain-voltage sweep from 0 to −40 V is performed at a constant gate-voltage V_G of −20 V. The source-drain-current I_{SD} is recorded and the measurement cycle repeated continuously during the pentacene deposition for up to several hours.

Selected conductance measurements with various degrees of pentacene coverage are presented in Fig. 2(a). For different pentacene thicknesses, we observe an increasing hole conducting TFT behavior with a distinct saturation. The transconductance curves for the off-to-on and the subsequent on-to-off gate-sweep for two different thicknesses are shown in Fig. 2(b). The extrinsic mobility μ_{ext} and the threshold voltage V_T are determined from the saturation regime.[7] The hysteresis V_{Hys} is calculated from the difference of V_T between the off-to-on and the subsequent on-to-off gate-sweep. At the early stage of pentacene deposition (1.5 ML) μ_{ext} of the transistor is smaller, V_T is more negative and V_{Hys} is larger compared to the same TFT covered by a thick pentacene film (25 ML).

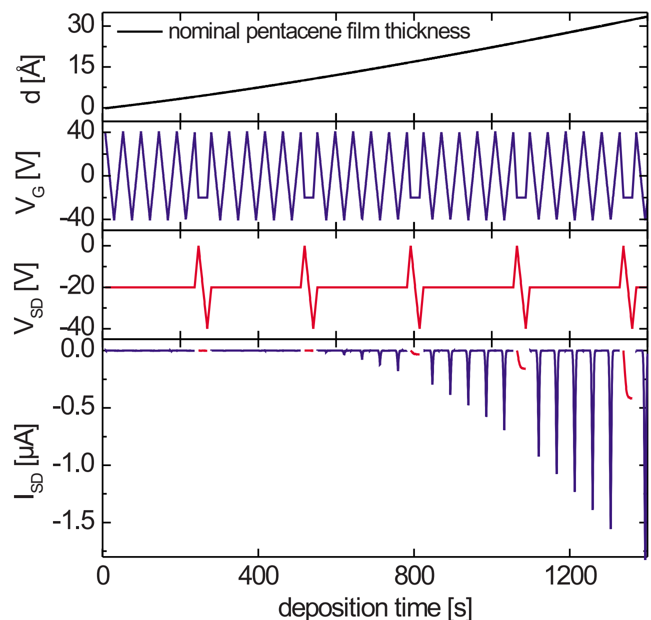

FIG. 1. (Color online) *In situ* measurement scheme. During pentacene deposition, the source-drain-current is continuously measured while gate- and source-drain-voltage sweeps are performed. One measurement cycle consists of five gate-voltage sweeps followed by a single source-drain-voltage sweep. This measurement scheme is repeated during the pentacene deposition time for up to several hours.

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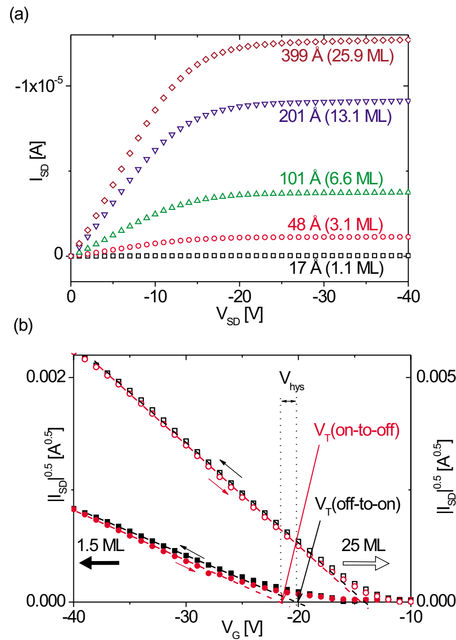

FIG. 2. (Color online) Conductance and transconductance measurements for selected pentacene thicknesses for a single TFT. (a) Conductance measurements at $V_G=-20$ V for five different pentacene film thicknesses recorded during pentacene deposition. (b) Off-to-on- and on-to-off gate-sweeps at $V_{SD}=-20$ V at a nominal pentacene film thickness of 1.5 ML (filled symbols) and 25 ML (open symbols), respectively.

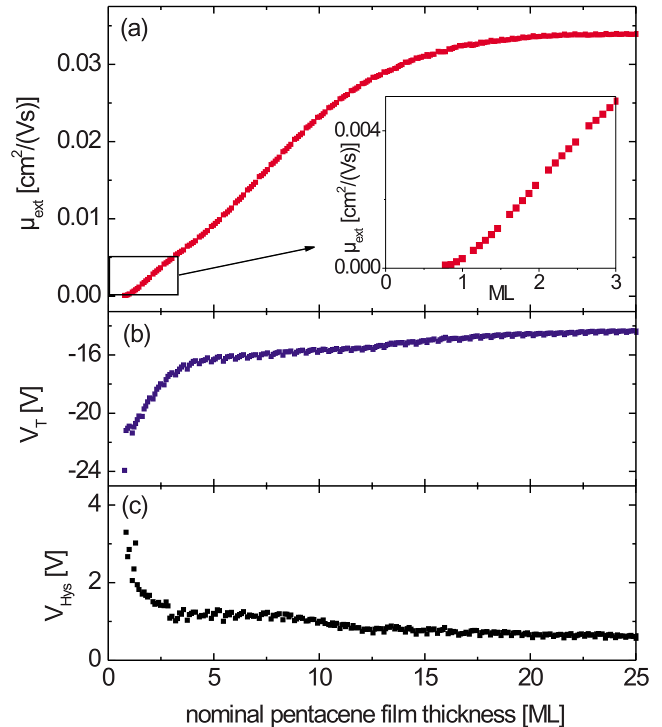

FIG. 3. (Color online) Pentacene film thickness dependency on transport characteristics for the same TFT as in Fig. 2. (a) The mobility increases to 0.03 cm^2/V s during the growth of the first 20 ML. (b) The threshold voltage shifts during the deposition of the first 4 ML to more positive values before it starts to saturate. (c) The hysteresis decreases rapidly until the film thickness has reached a nominal thickness of 4 ML.

Figure 3 shows the pentacene thickness dependence of the mobility, the threshold voltage and the hysteresis up to 25 ML. The first source-drain-current signal is measured at a pentacene coverage of about 0.7 ML [see Fig. 3(a)]. As pentacene initially grows layer-by-layer,[12] this is expected from percolation theory which predicts that the percolation threshold for a two-dimensional-growth is at about 0.66–0.68 ML (Refs. 13 and 14) depending on the shape of the nucleating islands, as observed experimentally.[8,9] The calculated extrinsic mobility increases during pentacene deposition of the first 20 ML and then saturates at about $\mu_{ext}=0.03$ cm^2/Vs. There are considerable sample variations of the mobility saturation thickness. Samples with high mobilities saturate earlier (our best performing transistor with $\mu_{ext}=0.27$ cm^2/Vs saturates at about 4 ML) than samples with inferior mobility that sometimes do not saturate even for thicknesses exceeding 40 ML. These variations indicate that the measured mobilities in our transistors is dominated by extrinsic influences such as contact properties or grain boundaries.[15–17]

Unlike the very sample-specific mobility saturation thickness, the threshold voltage evolves very similar for all transistors [see Fig. 3(b)]. During the growth of the first 4 ML the threshold voltage shifts, then saturates and remains constant. The subsequent slight increase is probably caused by bias stress.[18] The initial shift during growth can be explained by the filling of deep volume trap states, which increase in total number with film thickness. Since this shift is positive during the pentacene growth, these trap states capture electrons,[19] not holes.[20] As the pentacene film grows thicker, more and more electron trap states are filled by electrons thus negatively charging the pentacene film. Consequently, a more positive gate voltage is needed for compensation, which results in a positive threshold voltage shift, as observed. Using

$$n_{e^-}[x]=\frac{C_i}{e}\times(V_T[x]-V_T[x-1]), \tag{1}$$

where e is the elementary charge, $n_{e^-}[x]$ the area density of filled electron volume traps between a nominal film thickness of $(x-1)$ ML and x ML, and $V_T[x]$ the threshold voltage at a nominal thickness of x ML, we obtain electron trap densities of $n_{e^-}[2]=2.5\times10^{11}$ cm^{-2}, $n_{e^-}[3]=2.1\times10^{11}$ cm^{-2}, and $n_{e^-}[4]=1.0\times10^{11}$ cm^{-2}. As the threshold voltage with no deposited pentacene cannot be determined from the transfer curves, it is not possible to calculate the trap density for the first ML. Beyond a nominal pentacene film thickness of 4 ML, these electron trap states probably still form but are not filled, as these states are beyond the Debye length of the transistor channel.

Similar to the threshold voltage, the hysteresis also saturates at 4 ML [see Fig. 3(c)]. However, the hysteresis, that has been discussed in the context of shallow traps,[21] decreases during pentacene deposition from approximately 3 V at 1 ML to 1 V at 4 ML. As shallow volume traps should lead to an increase of the hysteresis during pentacene growth, they cannot account for this behavior. Therefore, we propose that the shallow trap states exist predominantly at the surface of the pentacene film. These trap states could arise from molecular sliding[22] or in general from local distortions of the molecular arrangement at the surface. If these surface traps are beyond the Debye length, they can neither be filled nor be emptied by the gate voltage, thus they do not contribute to the hysteresis. Beyond a nominal thickness of 4 ML it is apparent that the complete surface of the pentacene film is located beyond the Debye length as the hysteresis remains constant. Whether the shallow trap states within the Debye

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length are filled by holes or electrons cannot be distinguished by our measurements. Since both the threshold voltage and the hysteresis saturate at a nominal pentacene film thickness of about 4 ML, we conclude that the potential landscape of the TFTs converges for this coverage. Since pentacene does not strictly grow in a layer by layer fashion beyond the first ML,[12] a nominal thickness of 4 ML corresponds to a completion of 2–3 ML of pentacene, i.e., the second and maybe to a lesser extent the third ML of pentacene seem to be the final MLs that contribute to the formation of the channel.

In conclusion, both the threshold voltage and the hysteresis of our transistors saturate during pentacene growth at a nominal thickness of 4 ML, which shows that the potential landscape of the TFT channel converges for this coverage. Filling of electron volume trap states can explain the threshold voltage shift while the decrease in the hysteresis suggests the existence of shallow trap states located at the free pentacene surface. In contrast, the mobility saturates beyond 4 ML with large sample to sample variations, indicating that it is dominated by extrinsic limitations. These results are important for determining the minimum pentacene thickness for optimized transistor performance.

The authors gratefully acknowledge financial support from the Deutsche Forschungsgemeinschaft (Grant No. DFG Ni 632-4-1), the Center for NanoScience (CeNS), and the Nanosystems Initiative Munich (NIM).

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