4th International Workshop on Quantum Functional Devices (QFD2000)
November 15-17, 2000, Kanazawa, Japan

Manipulation of electrons in nanostructured semiconductors

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Nowadays single-electron devices are believed to be one of the top-candidates to replace standard Complementary Metal Oxide Silicon (CMOS) transistor technology at the end of the conventional semiconductor roadmap. Here, we present a brief overview on the manipulation of electrons in nanostructured semiconductors, especially in silicon with particular emphasis on different realizations of single-electron tunneling devices. Silicon-based fabrication technology further allows the use of the manufacturing processes already established in semiconductor industry. Moreover, the use of Silicon-on-Insulator (SOI) films allows the lithographic definition of the currently smallest structure sizes, which are crucial for the room temperature operation of single-electron devices. Lateral structuring of highly doped silicon films allows us to observe quasi-metallic Coulomb-blockade oscillations in shrunken wires where no quantum dot structure is geometrically defined. Embedding quantum dot structures into the inversion channel of a silicon-on-insulator field-effect transistor Coulomb blockade up to 300 K is observed. In contrast to the quasi-metallic structures, in these devices the influence of the quantum mechanical level spacing inside the dot becomes visible. As an outlook, we finally show freely suspended single-electron devices. Since dissipation can be highly suppressed in these novel devices, they might be especially suited for future applications in single-electronics.

Currently, several technologies are investigated in order to overcome the problems arising from scaling device dimensions down to or even below 10 nm. Especially single-electron devices such as single-electron transistors (SETs) are believed to be able to replace standard MOSFETs in this nanoscale regime. However, two conditions must be satisfied to successfully integrate single-electron devices in standard technology: Firstly, the devices have to work at room temperature, which requires that their geometrical dimensions are on the order of 5 nm and, secondly, the choice of silicon for fabricating the structures is necessary for compatibility and integrability. Especially silicon-on- insulator (SOI) materials, where a thin film of crystalline silicon is located on top of an insulating layer separating the silicon film from the underlying substrate, are the most promising candidates for such silicon-based SET structures. Up to now, several different types of single-electron devices based on SOI or similar structures have been proposed and realized [1–3], leading to first SETs working at room temperature [2, 4].

Single-electron tunneling through a quantum dot occurs when the electron island is weakly coupled to source and drain leads. In order to maintain discrete energy states inside the dot, the energetical uncertainty due to lifetime broadening has to be much smaller than a typical interaction energy in the dot. Since electron flow onto the dot is suppressed by Coulomb repulsion (Fig. 1a) this energy scale will be the Coulomb charging energy $E_C = e^2/C$, with C being the total capacitance of the electron island. Approximating the lifetime by a RC time-constant leads to the condition for single-electron flow via source and drain contacts: $R >> h / e^2$ with R being the resistance of the tunnel contacts and h Planck's constant.

In other words, electrons have to tunnel successively onto and from the dot in order to resolve single-electron effects. On the other hand, tunneling through the electron island can only occur when the source and drain chemical potential $m_{S(D)}$ is aligned to one quantum dot state (Fig. 1b). The electron energy $E(N)$ contains both the electrostatic Coulomb energy $(Ne)^2/2C$ as well as the purely quantum mechanical contribution ΣE_i where the E_i are the single particle energy levels within the dot [5]. When a small quantum dot is occupied with only a few electrons, the quantum mechanical contribution dE_N can become significant and strongly alter the periodicity of the Coulomb blockade (CB) oscillations. For silicon dots in the inversion layer of SOI-MOSFETs, dE_N can be comparable to the Coulomb energy and therefore no periodicity of the observed conduction peaks can be expected. In the opposite, i.e. metallic limit, the electron island is occupied with a large number of electrons. Transport through such a system is dominated by the Coulomb repulsion of the electrons. For silicon, the metallic limit can be practically reached by using a very high doping level. Since the conductance peaks are equidistant in this case, switching the electron island from a conducting to a non-conducting state by a proper change of gate voltage can be utilized to operate the device as a "single-electron transistor" (SET). In contrast to conventional MOSFETs a change of the island's charge by e just requires one more electron on the gate. This can be easily deduced from a simple capacitor model of the SET where the gate is connected to the electron island via the capacitance C_G. Nonlinear transport characteristics can be obtained, when a voltage difference V_{SD} is applied between the source and drain contacts which is high enough to drive the system out of the linear response regime. In the nonlinear regime, the Coulomb blockade can be lifted and several quantum dot levels may contribute to transport. Schematic nonlinear I_{SD} - V_{SD} characteristics are displayed in (Fig. 1d) for the CB case (gap around zero V_{SD}) and for single electron tunneling (Ohmic behaviour). Since a finite difference of the source and drain electrochemical potential allows electrons to flow through the dot as long as an energy level is situated within this "transport window" (Fig. 1c), the conductance peaks broaden.

We start our fabrication by doping the SOI wafers by ion implantation of As. For the highly doped SET devices a uniform doping of the whole wafer is employed. In order to fabricate inversion-MOS structures, we mask the areas of the active MOS structures by conventional photoresist. When employing low-energy electron-beam lithography with calixarene [6] to fabricate SET structures in SOI films, the exposed resist film is used as an etch mask for a reactive ion etching process (RIE) which removes the unprotected silicon layer down to the SiO_2. Since the calixarene resist has a lower etching rate in the CF_4 plasma used than silicon, the masking is suitable for structuring SOI films up to a thickness of about 50 nm. Large contact regions are protected by a photoresist masking during the RIE process. We subsequently grow a thin thermal gate oxide at a temperature of 950 ^{o}C in order to passivate the etched structures and to anneal etching damage at the structure surfaces. We then deposit a second oxide film either by chemical vapor deposition or by sputtering and provide a metallic top gate by evaporation or sputtering. This fabrication process can either be applied to uniformly highly n-doped SOI wafers or to slightly p-doped layers suitable for inversion-MOS-structures, where only the source and drain regions are highly n-doped by selective implantation.

In the following, we briefly present several approaches to the fabrication of reliable room temperature operating silicon-based single-electron tunneling devices. (i) In highly doped silicon nanowires ($N_D = 10^{20}$ cm^{-3}) in dual gate configuration the potential inside the wire can be tuned independently by variation of the top and the side gate voltages [7]. In Fig. 2, the conductance $g = dI_D/dV_{SD}$ of a silicon wire is plotted versus the side gate voltage V_{SG} with the top gate voltage kept constant near the pinch-off. This allows to minimize the controlling side gate voltage which is of special importance for possible applications of these devices

within integrated circuits. Here almost periodic CB oscillations can be resolved. However, both the peak amplitudes as well as the exact peak positions differ between subsequent gate sweeps. Single-electron effects remain visible only weekly up to temperatures of about 200 K. (ii) Furthermore, we fabricated silicon nanowires from SOI-films with even higher doping concentration. In these quasi-metallic structures (N_D = 10^{21} cm^{-3}) CB oscillations with a clear periodicity are observed. The oscillations remain visible up to temperatures of almost 100 K (Fig.3) [8]. (iii) Another kind of single-electron tunneling device can be realized by lateral confining of an inversion layer in an SOI-MOSFET (metal oxide semiconductor field effect transistor) [9]. The clear deviation from regular CB oscillations of a small quantum dot with lithographical diameter of 20 nm indicates the strong influence of energy quantization. In greater detail we examined the temperature dependence of the non-linear charateristic. A clear CB gap in the conductance is found even at room temperature (Fig. 4). Since in this device CB should be visible up to temperatures of $T = E_C/(2k_B)$ = 310 K, this finding is in good agreement with the theoretical expectations. (iv) Underetching of lithographically defined SOI-nanostructures leads to suspending of these devices and therefore to a thermal decoupling from the silicon substrate. The buried oxide can be easily removed locally in buffered hydrofluoric acid. The exact fabrication process of these devices is described in detail elsewhere [10]. In Fig. 5, an SEM-micrograph of a side gated suspended silicon wire is shown. First results on the non-linear transport characteristic will be discussed.

SUMMARY Here we present measurements on single-electron devices fabricated out of highly doped SOI, devices realized in quasi-metallic SOI and devices embedded in inversion field-effect structures. They all show single electron effects such as Coulomb blockade. The electrical properties of the different single-electron devices are compared. Silicon quantum dots in SOI-MOSFETs are the most promising candidates for room-temperature operation, whereas highly doped and especially quasi-metallic structures allow a better control of the periodicity of the conductance oscillations. We have further demonstrated a novel kind of silicon nanostructure: the suspended SET. Here single-electron effects in thermally decoupled nanostructures can be observed. These devices allow a new class of experiments investigating the combination of phonon quantization and single-electron tunneling.

ACKNOWLEDGEMENT Financial support from the BMBF (contract number 01M2413) and from the DFG (Schwerpunktprogramm ‘Quanteninformationsverarbeitung’) is gratefully acknowledged.

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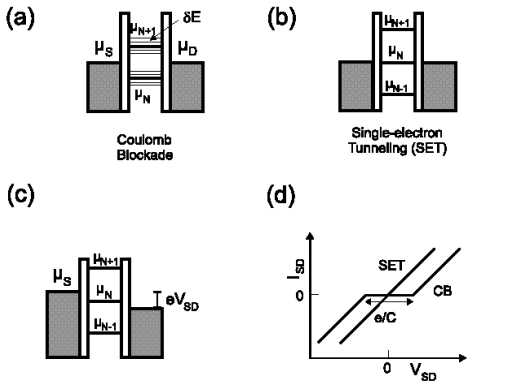

Figure 1: (a) If the chemical potentials of the source and drain leads are not aligned to an energy level inside the electron island (Coulomb blockade), no current can flow through the dot. The energy levels are split in a series separated by the single particle energy dE_N as sketched in (a). Only when the chemical potentials are aligned to one energy level (single-electron tunneling) (b) or if one energy level lies in the gap between the chemical potentials of source and drain (c) current can flow. These two effects lead to the observation of the source-drain characteristic (d).

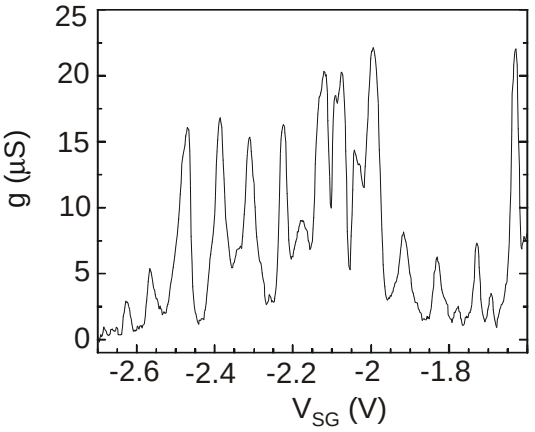

Figure 2: Coulomb blockade oscillations in a highly doped silicon nanowire. The top gate voltage in this measurement is V_{TG} = 17.5 V, which allows low side gate voltages to control the CB oscillations.

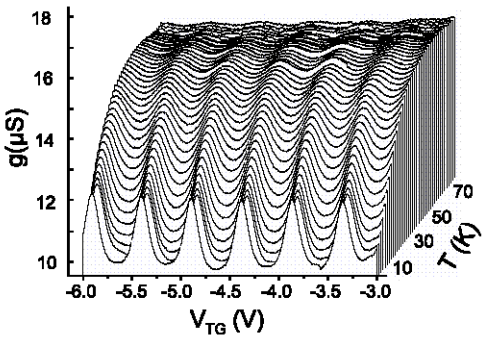

Figure 3: Temperature dependence of the CB oscillations in quasi-metallic nanowires

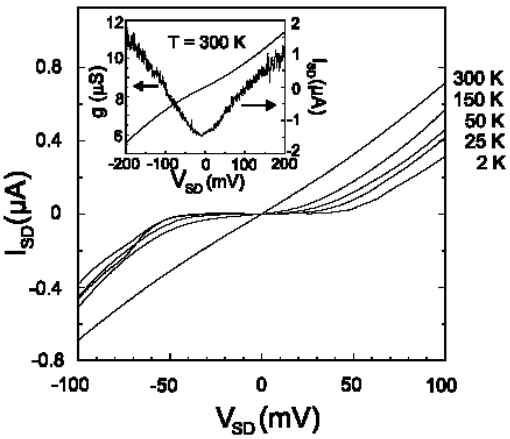

Figure 4: Temperature dependence of the non-linear characteristic of an inversion tunneling device.

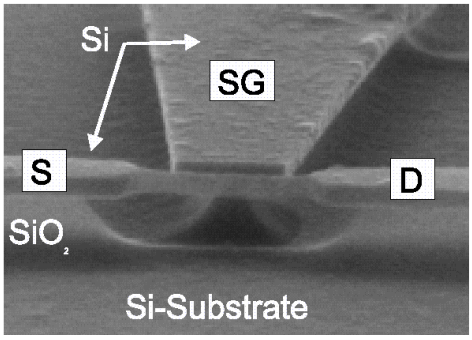

Figure 5: SEM micrograph of a suspended silicon nanowire with a side-gate.