Single-crystalline silicon lift-off films for metal–oxide–semiconductor devices on arbitrary substrates

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We present a technique to mount single-crystalline silicon thin films on arbitrary substrates. We demonstrate in detail the preparation of a 190-nm-thin silicon metal–oxide–semiconductor field-effect transistor (MOSFET) on a silicon-on-insulator film lifted from its substrate and bonded to quartz. Functioning of this hybrid MOSFET on a rigid surface at room temperature is demonstrated. © *2000 American Institute of Physics.* [S0003-6951(00)02030-1]

Silicon semiconductor structures are nowadays the main components of microelectronic circuits. Complementary metal–oxide–semiconductor (CMOS)-based integrated circuits on bulk silicon substrates are the basis for almost every logic application in semiconductor technology. Silicon-on-insulator (SOI) materials, realized in separation by implantation of oxygen (SIMOX) or smart-cut wafers,[1] additionally open a new field of radiation-hard, ultrafast, and low-power-consuming silicon devices. This technology is already finding its way into industrial applications.[2] Recently, also the use of silicon-based thin-film transistors (TFTs) has attracted broad interest in the emerging field of large-area electronics. Realizing silicon-based TFTs on thin foils using plasma-enhanced chemical-vapor deposition (CVD) of hydrogen-passivated, amorphous silicon (*a*-Si:H) recently demonstrated the usability of these TFTs for rollable and foldable film-on-foil electronics.[3,4]

Combining silicon microelectronics on crystalline, high-quality thin silicon films with the properties of arbitrary substrates could presumably open prospects in this field of large-area electronics such as charge-coupled-device detectors as well as fast integrated circuits. An approach combining single-crystalline semiconductor films with almost arbitrary substrates uses the selectivity of wet-chemical etchants to underetch and lift thin semiconductor films. These films are subsequently bonded to the new substrate by van der Waals forces (vdW bonding) only. Thin $Al_xGa_{1-x}As$ films have been already bonded onto various substrates using epitaxial lift-off technology (ELO).[5–7] Employing this technique in the field of microelectronics, only GaAs metal–semiconductor field-effect transistors on silicon[8] and InP,[9] AlGaAs/GaAs heterojunction bipolar transistors on silicon,[10] and high electron mobility transistors on quartz and sapphire[11] have been realized. All these investigations indicate no loss of film quality during the ELO process. Further work has already shown the ability to bond $Al_xGa_{1-x}As$ thin films to curved surfaces like small glass and plastic rods.[12] Regarding the technological importance of silicon, also single-crystalline silicon layers being placed on curved or even flexible substrates are highly desirable. Due to the use of CVD-defined amorphous silicon in Ref. 3, fast CMOS–silicon devices with low-leakage current and low-threshold voltage, as well as integrated circuits, cannot be realized in these curved films. Here, we present a silicon-based lift-off (LO) process, where a thin SiO_2 sacrificial layer under the active semiconductor layer is selectively removed by wet-chemical etching, in order to produce single-crystalline silicon LO films. Although, techniques of fabricating bonded silicon films are already applied by some companies,[13] the processing techniques for a silicon-based LO process are not documented in the literature. We demonstrate the usability of the LO technique for silicon by bonding a 190 nm thin silicon film on quartz and fabricating a *p*-channel enhancement field-effect transistor on this quasimonolithical hybrid structure.

The best-suited structure for silicon-based LO processes is found in state-of-the-art SOI wafers, where the high-quality top single-crystalline silicon film is located on a thin SiO_2 layer. For technical reasons, we used postprocessing[7] as exemplified in Fig. 1. Hereby the silicon MOS structures are defined after bonding. Our starting SOI structure consists of a 190-nm-thick boron-doped SIMOX film with a resistivity of about 20 Ω cm on top of a 360-nm-thick insulating SiO_2 film (a). Since the etching rate of silicon depends strongly on the doping level and on the buffering of the etchant, we used SIMOX substrates with a low doping level ($\sim 7 \times 10^{14}\,cm^{-3}$) that are also commonly found in today's CMOS devices. For processing, the wafer was sown into pieces with a lateral size of $5 \times 5\,mm^2$. The samples were then covered with a thick ($\sim$200 μm) protective wax Apiezon-W (Apiezon Products, M&I Materials Ltd., P.O. Box 136, Manchester, M60 1AN, U.K.). First, the Apiezon-W is heated to 65 °C and a number of wax drops are collected on the samples' surface. Heating the sample to 65 °C leads to a homogeneous distribution of the wax across the surface. Thinner layers can be realized by solving the Apiezon-W in trichloroethylene and by spinning of this solution. We then attached a small piece of Teflon or Apiezon-W (not molten) to the top of the protected chip in order to enable easy handling of the film with tweezers [Fig. 1(b)]. The SOI chip with its handle is then mounted in a rack with which the chip can be minutely dipped into the etchant with the help of a micrometer screw. During the subsequent etching of the SiO_2 sacrificial layer in HF (48%) at a tem-

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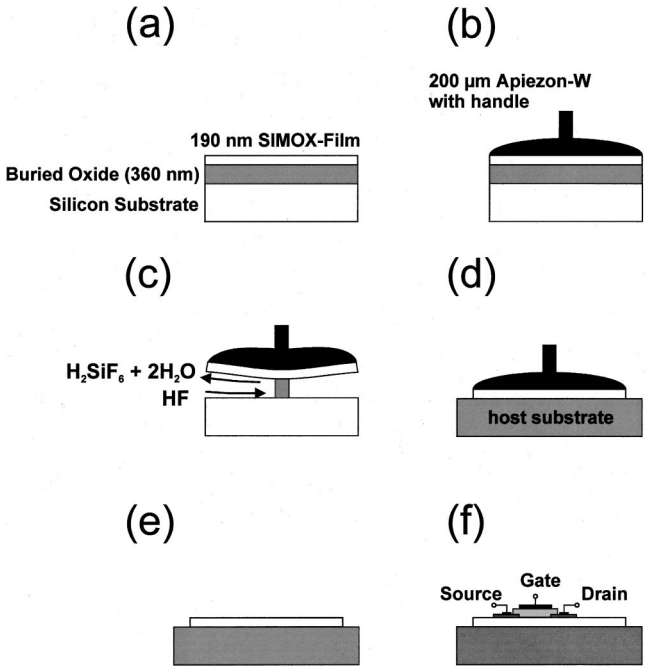

FIG. 1. Schematically shown is the process of fabricating silicon LO films: Starting from a slightly boron-doped silicon-on-insulator structure (a), the silicon film is covered by a thick Apiezon-W film protecting the surface (b) and subsequently underetched in diluted HF (c) and attached onto an arbitrary substrate by van der Waals forces (d). The Apiezon-W is removed (e) and an enhancement MOSFET is defined (f).

perature of 25 °C, the underetching of the SOI film proceeds from the sample edges towards its center until finally the carrier substrate floats in the etchant [see Fig. 1(c)].

We found no significant deviation in the lateral etching rates compared to the vertical etching rates of buried oxide. Lowering the HF concentration to 10%, a reduction of the etching rate by a factor of about 20 is found, but no qualitative variation of the film's properties. For the temperature dependence of the underetching, we observed the well-known Arrhenius-type behavior (see Fig. 2), indicating that underetching in the SOI system is not limited by the diffusion of reaction species in the gap formed between substrate and film. This is of great importance, since it allows us to underetch also larger SIMOX films with an only linear increase in etching time with chip diameter. For wafer-scale applications, the SOI wafers can be separated in single chip areas by etching grooves until the SiO_2 sacrificial layer is reached. As seen, the etch rate can also be enhanced by increasing the temperature of the HF etchant.

After underetching the silicon film, which is covered by the thick carrier layer of Apiezon-W, the film is picked up at its handle and placed on the substrate of choice; the still remaining water film on the substrate's back enables us to slide the device into the desired position [Fig. 1(d)]. The film bonding itself is performed in air without any additional pressure applied. For large area films ($20\times20\,\mathrm{mm}^2$) it is recommended to use a mounting rack, allowing a fine approach with a micrometer srcew. In order to bond films onto curved substrates, thinned Apiezon-W layers can be applied, which are then gradually removed by trichlolorethylene, thus lowering the stress.[12] As the hydrophobic film is mainly fixed on the substrate by van der Waals forces, it can be attached to rigid as well as flexible substrates.

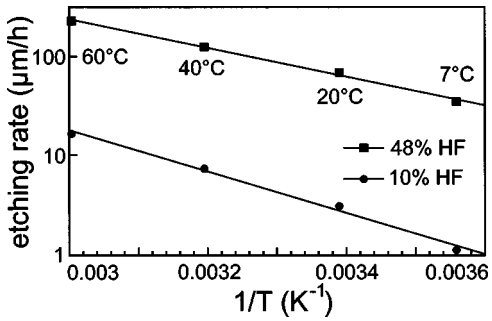

FIG. 2. Temperature dependence of the underetching rate in 48% HF and 10% HF. The common Arrhenius-type plot and no significant deviations from the vertical etching rates are found.

The work of adhesion W_{vdW} for silicon due to van der Waals forces can be expressed as[14]

$$W_{\mathrm{vdW}}=\frac{A}{12\pi d_{\mathrm{vdW}}^2}, \tag{1}$$

where d_{vdW} denotes the contact distance and A is the Hamaker constant with $A\approx1.6\,\mathrm{eV}$ for Si.[15] Taking $d_{\mathrm{vdW}}\approx0.5\,\mathrm{nm}$ one calculates an adhesion energy of 29 $\mathrm{mJ/m}^2$. The role of hydrogen bonds, with adhesion energies in the range of 90–350 $\mathrm{mJ/m}^2$,[14] can be neglected as hydrogen bonds are usually formed at hydrophilic silicon surfaces containing a large number of hydroxyl groups, which are not present after HF etching. The deposited silicon films are now tempered at 50 °C for 2 h to increase the bonding strength and to remove the remnants of the wet etch step. The Apiezon-W is subsequently removed in trichloroethylene, leading to the final silicon single-crystal-film structure, which is tempered at 90 °C for at least 10 h in order to obtain a further increase in bonding strength [Fig. 1(e)].

Atomic-force microscopy investigations revealed no significant deviation of the step height at the edge of the bonded silicon film compared to the original silicon film thickness, demonstrating that no thinning of the silicon film during the HF etch takes place. In addition, we determined the surface roughness, which displayed no significant increase during the LO process.

In order to investigate the electronic properties of the LO-silicon films, we prepared an accumulation FET in a film bonded to quartz as a substrate (LO-MOSFET). Since we were forced to avoid high-temperature steps in our postprocessing technique [see Fig. 1(f)], the gate oxide in our MOSFET was realized by sputter deposition of 120 nm SiO_2.[16] We used 50-nm-thick Pt regions for the definition of source and drain contacts on the *p*-type silicon film.[17] A top gate is defined by optical lithography and thermal evaporation of 100 nm Al.

The final device is shown in Fig. 3 in a top view: The completed LO-MOSFET can be seen in between the metallic gate and bond pads, which were subsequently prepared by evaporation of 100 nm Al. The lateral dimensions of our device with a gate channel length L of 7 μm and a gate width W of 20 μm can certainly be lowered in future device applications. We achieved lateral gate dimensions in silicon single electron transistors of only 15 nm.[18]

In Fig. 4 the transfer characteristic I_D vs V_G at $V_D=50\,\mathrm{mV}$ and the output characteristic I_D vs V_D at a fixed

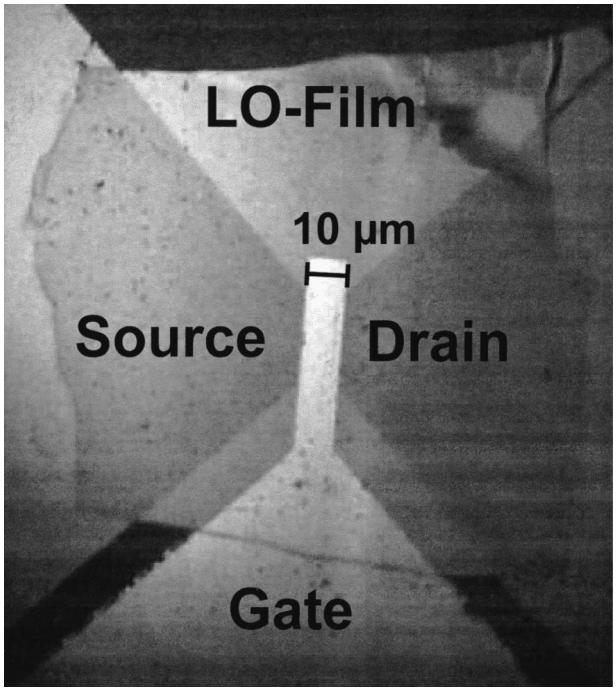

FIG. 3. Micrograph of the realized LO-MOSFET: Pt pads were used for source and drain contacts. The LO film was laterally patterned in order to form a mesa structure in the active region for device isolation.

gate voltage of the LO-MOSFET is shown (I_D and V_D are the source–drain current and source–drain voltage, respectively). Estimating the mobility from the linear region of the *IV* characteristics in Fig. 4 yields $\mu = I_D L/(C_{ox} W V_D V_G) \approx 0.01\,\mathrm{cm}^2/\mathrm{V\,s}$. Hereby, it is assumed that all the source–drain voltage drops across the conducting channel. However, we found in various measurements on MOSFETs fabricated on not-lifted SIMOX films of the same wafer that the contact resistance between the Pt pad and the silicon film is very high. This implies that most of the drain voltage drops across the source and drain contacts. As a consequence, a much higher mobility comparable to that in conventional SOI films can be assumed. Moreover, it cannot be excluded that the effective doping concentration in the SOI film is somehow lower than determined for the bulk of the SOI wafer. Especially the relatively high oxygen concentration in SIMOX films can lead to a partial compensation of *p*-type doping and, therefore, lower the hole concentration inside the bonded film.[19] Furthermore, a lower *p*-type doping level would cause even higher contact resistances in our simple Pt/*p*-Si Ohmic contact. Although the obtained mobility is far from perfect, the traces presented demonstrate the realization of a MOSFET operating on a silicon LO film. Naturally, the performance can be improved by using better gate oxides, enhancing the film's homogeneity and shrinking the gate dimensions.

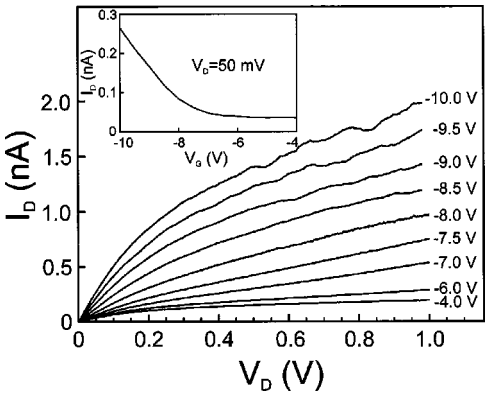

FIG. 4. Output characteristic I_D vs V_D at fixed gate voltages and transfer characteristic [I_D vs V_G (inset) for the silicon thin-film *p*-channel LO-MOSFET ($T = 300$ K)].

In summary, we presented the realization of silicon-based single-crystalline thin-film MOSFET structures on a quartz substrate. Since this technology provides a technique to attach single-crystalline-silicon films onto arbitrary and even flexible substrates, the abilities of today's TFT devices could be further increased by incorporating high-speed CMOS technology. This combination of thin, crystalline silicon films with nearly arbitrary substrates also allows us to integrate electronic with nanomechanical devices operating at radio frequencies.

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