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Single-electron effects in highly doped polysilicon nanowires

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Abstract

We investigate silicon-based single-electron transistors in thin layers of highly doped recrystallized amorphous silicon. After rapid thermal annealing polysilicon grains have been found with sizes of about 25 nm acting as electron islands. Applying high-resolution electron-beam lithography we have fabricated nanowires with width down to about 10 nm in the polycrystalline silicon films. Single-electron effects in the non-linear source–drain characteristics up to temperatures of about 25 K have been observed. © 2002 Elsevier Science B.V. All rights reserved.

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1. Introduction

Recently, single-electron transistors (SET) realized in silicon-on-insulator (SOI) were found to exhibit Coulomb blockade effects up to room temperature [1–3]. Both, SETs embedded in inversion-field effect structures [1–4], as well as highly doped silicon nanowires where a gate voltage can change the chemical potential inside the wire were used [5–8]. However, in particular in highly doped SOI-nanostructures the origin of the electron island formation is not yet fully understood. Doping fluctuations as well as segregation effects can be made responsible to cause a serial arrangement of multiple tunnel junctions (MTJ) inside the nanostructures. Irvine et al. [9] first used highly doped polycrystalline silicon films to fabricate SET-devices. Also amorphous, recrystallized silicon was used by this group [10]. Since the size of the polysilicon grains can be adjusted during an annealing step to be about 20 nm, a controllable formation of multiple dot structures in a polysilicon nanowire can be achieved. Yano et al. [11] observed single-electron effects in ultrathin polycrystalline wires embedded in a metal–oxide–silicon field effect structure. Electron transport turned out to be dominated by thermal emission. Thus, making the wire highly conductive by applying a positive gate voltage, an Arrhenius type behaviour of the conductance was observed. Also the use of highly doped polycrystalline silicon films as an application for floating dot memory has attracted much interest in the last few years [12–14].

Here, we present results on Coulomb blockade experiments performed on highly As-doped nanowires structured in sputtered amorphous and recrystallized silicon films. In addition, we investigate the electronic properties of these nanowires in high magnetic fields up to $B = 12$ T. Since sputtering of amorphous silicon

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(a-Si) in combination with rapid thermal annealing (RTA) is a less expensive fabrication method than the use of high quality SOI-material to form highly doped SET-structures, this fabrication process is of importance for future device applications.

2. Fabrication

On a standard n-type silicon wafer covered with a 500 nm thick thermal oxide a 40 nm thick a-Si layer was deposited by radio frequency (RF) sputtering in an Ar-plasma [15]. In order to produce a-Si films with highest possible film qualities the variation of different sputtering parameters such as RF-power, Ar-pressure and substrate bias was investigated. The qualities of these different films were then examined both by measuring the surface roughness with an atomic force microscope (AFM), as well as by investigating the refraction index by optical ellipsometry. The optimum sputtering conditions as judged from optical density and surface morphology lead to a sputtering rate of 6.6 nm/min.

Subsequently, the a-Si-films were highly n-doped by ion-implantation of As with a dose of 2×10^{15} cm^{-2} at an ion energy of 20 keV. These parameters led to a nominal doping level of these a-SOI-films of about 4×10^{20} cm^{-3}. High-temperature annealing performed in a RTA chamber served both, to activate the dopant atoms [16] as well as to recrystallize the a-Si layer [17,18] to form a polycrystalline silicon (poly-Si) film. In Fig. 1(a) the AFM-image of the surfaces of an ion-implanted but not yet annealed a-Si film is shown. Fig. 1(b) shows the surface annealed for 30 s at a temperature of 1000°C. Nanometer sized polysilicon grains are clearly visible. An average diameter of these grains is determined to be about 25 nm. The grain size increases both with longer annealing time as well as with higher annealing temperature. Since these poly-Si grains are intended to serve as single-electron islands in laterally structured nanowires, the annealing time has to be very short and properly controlled in order to guarantee small grain sizes. On the other hand, both electronic activation of the dopant atoms as well as the electronic quality of the nanocrystals increases with higher annealing temperature. Therefore, in our investigations we found an annealing duration of 30 s at a temperature of 1000°C to be a suitable compromise between small grain size and acceptable electronic qualities.

The highly doped poly-Si films were then laterally patterned by low-energy electron-beam lithography using the negative electron resist calixarene [19]. Reactive ion etching with CF_4 and evaporation of contact-pads completed the fabrication process. Fig. 2 shows a scanning electron-beam micrograph of one of our devices. In-plane sidegates were integrated in the poly-Si film in order to permit electrostatic control of the nanowire. Usually, single-electron structures in SOI-films can be passivated and further shrunk by thermal growth of a thin gate oxide [1]. In order to avoid preferential oxidation at the grain boundaries of the poly-Si nanowire [20] we abandoned this fabrication technique for the devices presented here. Due to this lack of a gate oxide only the sidegates were available to control the conductance of the wire. The samples were then mounted into a chip-carrier, attached onto a sample holder and characterized in the chamber of a variable temperature insert (VTI) allowing temperatures in the range between 1.5 and 250 K. The VTI was surrounded by a superconducting solenoid providing magnetic fields up to 12 T.

3. Measurements

We used standard lock-in techniques to measure the conductance $g = dI_D/dV_{SD}$—with I_D the drain current—of the nanowires as a function of applied source–drain bias V_{SD}, of a sidegate voltage V_{SG}, of temperature T and of the magnetic field B. Fig. 3(a) shows the conductance of a 25 nm wide, 40 nm high and 500 nm long poly-Si nanowire as a function of temperature. At low T a conductance dip around $V_{SD} = 0$ V is visible that can be attributed to the formation of multiple tunnel junctions (MTJ) formed in the polycrystalline structure [5,9]. This conduction dip at zero source–drain bias vanishes at temperatures of about 24 K. Applying a negative sidegate-voltage to the in-plane gate leads to a reduced conductance of the nanostructure. Nevertheless, we cannot deplete the device sufficiently for ensuring only weak electronic coupling between neighbouring silicon grains. Therefore, we are not able to observe

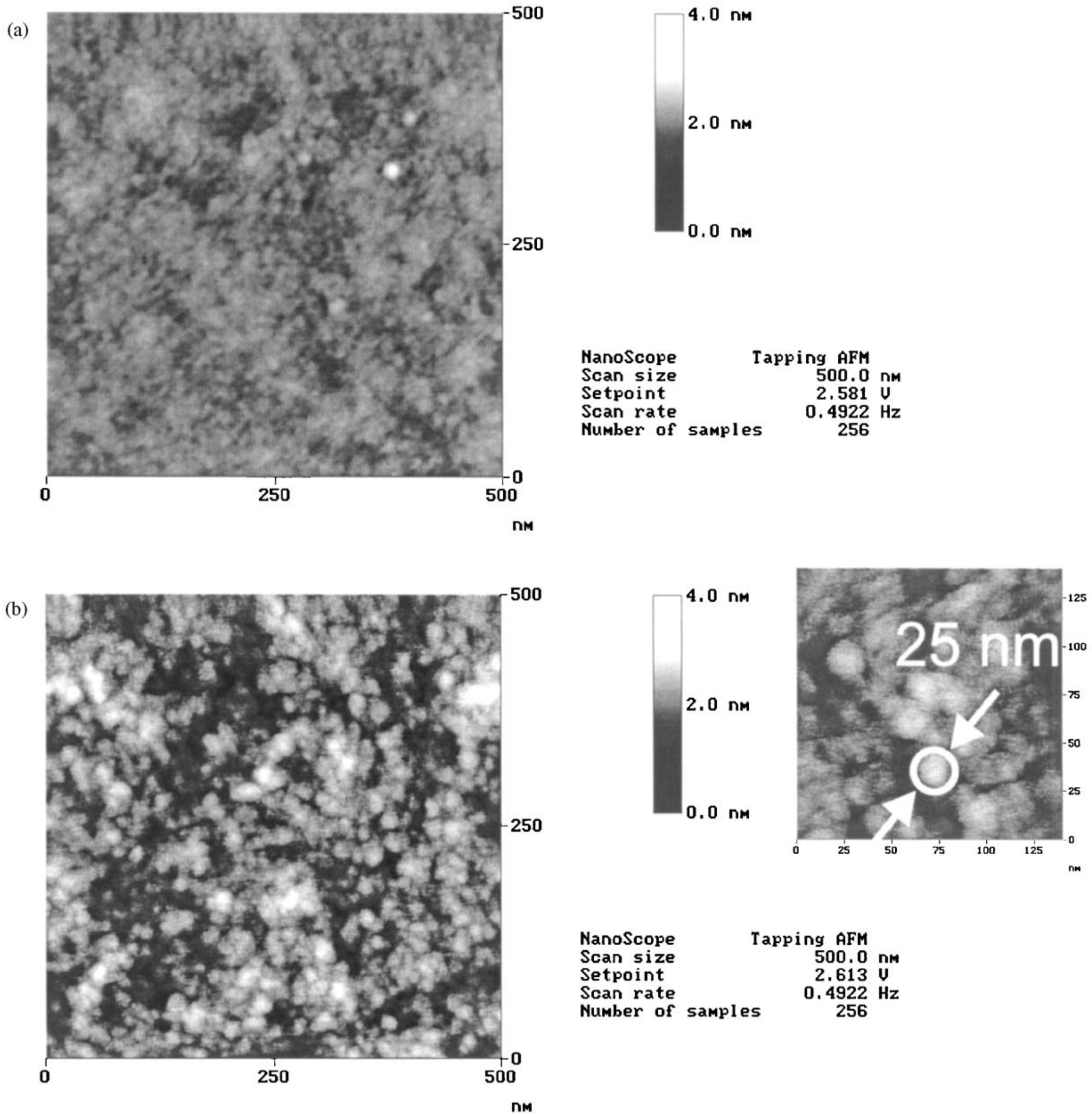

Fig. 1. (a) AFM-micrograph of a sputtered and ion-implanted a-Si film on an oxidized silicon wafer. The surface roughness is similar to that of the substrate-wafer. In (b) an AFM-scan of a recrystallized polysilicon film is shown. Polysilicon grains with diameters of about 25 nm are found (inset).

a conductance minimum at $g = 0$ as a function of V_{SD} and also only very weak conductance oscillations as a function of V_{SG} in contrast to monocrystalline, highly doped, fully depleted silicon nanowires [5,7].

In the inset of Fig. 3(a) the temperature dependence of g at $V_{SD} = 0$ V with an AC-sensing voltage of $V_{sd} = 100$ μV is shown. In contrast to the observation in Ref. [11] no activation type behaviour of the conductance can be found. In our structures the grain

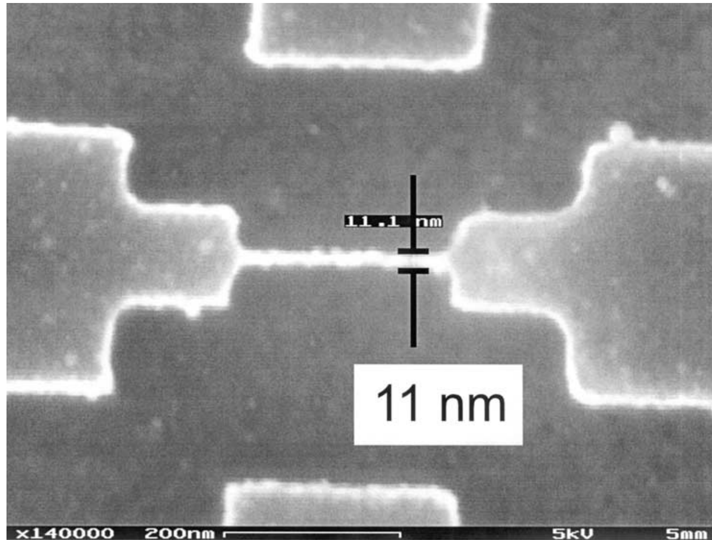

Fig. 2. SEM-micrograph of a 11 nm wide nanowire in a 50 nm thin polysilicon film defined by low-energy electron-beam lithography.

boundaries are saturated with As in contrast to the undoped polysilicon films, as stated in Ref. [11]. Presumably, thermal emission can therefore not be observed in the highly doped wires.

The number N of the tunnel junctions inside the nanowire can be estimated from the temperature dependence of the full-width at half-maximum (FWHM) of the conductance dip around $V_{SD} = 0$ V [21]. From the traces shown in Fig. 3(a) we derive $N \approx 12$ for the polycrystalline wire discussed here. Attributing one tunnel junction to one polysilicon grain inside the wire with a length of 250 nm we obtain a mean grain size of about 21 nm. This is in very good agreement with the AFM measurements shown in Fig. 1.

The magnetic field dependence of the conductance shown in Fig. 3(b) displays a decrease of the conductance dip but no complete reduction up to $B \approx 6$ T. This finding indicates a clear B-dependence of the effective tunneling barriers. Since this dependence turns out to be weak the confining potential inside the silicon grains can be assumed to be rather strong. Strikingly, the conductance minimum becomes deeper when increasing the magnetic field further and decreases again at $B > 11$ T. Deriving the Fermi-wavelength λ_F from the electron density one finds $\lambda_F \approx 4$ nm for a crystalline film. Taking that value for a simple approximation, one gets the classical cyclotron radius r_B for electrons in high magnetic field B perpendicular to the sample surface $r_B \approx 1$ µm/B [T]. The second minimum in the conductance at zero bias around $B \approx 10$ T therefore corresponds to $r_B \approx 100$ nm. Taking into account the crude simplifications in this evaluation, this value is comparable to the extensions of the poly-Si grains and is therefore ascribed to stronger electron confinement inside the grains at high magnetic fields.

4. Summary

In summary, we have fabricated single-electron devices out of highly doped, polycrystalline silicon films. These films were deposited on oxidized, standard silicon wafers by sputtering, doped by ion-implantation and recrystallized by RTA. The SET-structures were defined by high-resolution electron-beam lithography and dry-etching. Single-electron effects have been found up to temperatures of about 24 K. The non-linear source–drain characteristics displays an only weak dependence of magnetic fields up to $B \approx$ 12 T indicating a rather hard confinement potential inside the poly-Si grains.

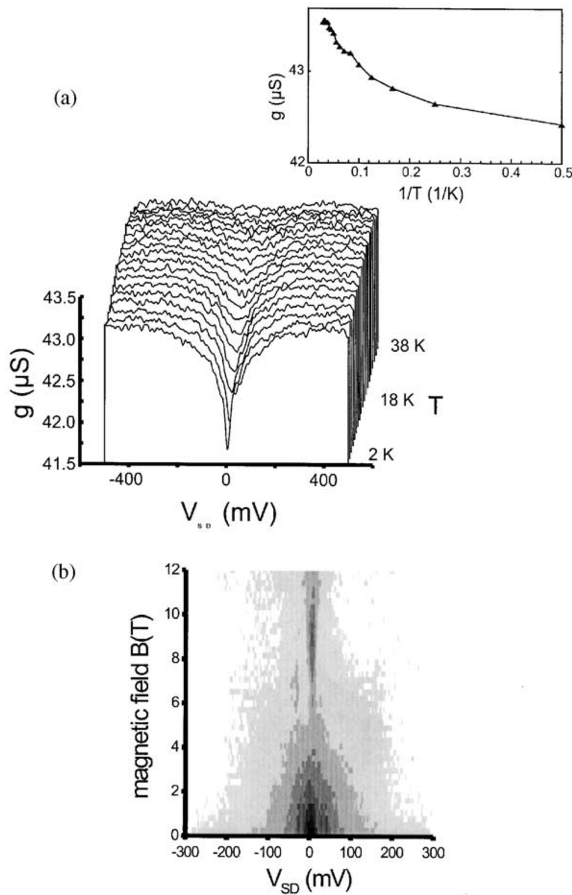

Fig. 3. (a) Temperature dependence of the non-linear source–drain characteristics of a 25 nm wide, 40 nm high and 500 nm long poly-Si nanowire. The inset shows the temperature dependence of the conductance at zero bias $V_{SD} = 0$ V. (b) Magnetic field dependence of the conductance at $T = 2$ K. A second minimum around $B \approx 10$ T is visible.

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