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Review

Coulomb blockade in silicon nanostructures

A.T. Tilke[a,*], F.C. Simmel[b], R.H. Blick[c], H. Lorenz[c], J.P. Kotthaus[b]

[a] *Infineon Technologies, Königsbrücker Street, 180, 01099 Dresden, Germany*
[b] *Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974, USA*
[c] *Center for NanoScience and Sektion Physik, Ludwig-Maximilians-Universität Munich, Germany*

Abstract

Today single-electron devices are believed to be among the top candidates to replace standard complementary metal oxide silicon field effect transistor technology at the end of the conventional semiconductor roadmap. In this review, we present a brief survey of different realizations of single-electron devices fabricated in silicon-on-insulator (SOI) films. Using a silicon-based fabrication technology allows the further utilisation of the manufacturing processes already established in semiconductor industry. Moreover, the use of SOI allows for the lithographic definition of the currently smallest structure sizes, which are crucial for the room temperature operation of single-electron devices. We start our review with a simple introduction into the physical concepts of single-electron tunneling, followed by a description of the nanolithographic preparation techniques which are used to define room temperature single-electron devices. Then, we present our latest measurements on the different types of single-electron devices treated in this review. As an outlook, we finally show first results on freely suspended single-electron devices. Since dissipation can be highly suppressed in these novel devices, they might be especially suited for future applications in single electronics.

Contents

*Corresponding author.
E-mail address: armin.tilke.drs@infineon.com (A.T. Tilke).

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1. Introduction

Since its invention in 1947 [1,2], the semiconductor transistor became the main component of modern computation and communications. The most striking new feature of silicon-based transistors was the possibility to develop integrated circuits (IC) [3] which led to an astounding component density of many millions of transistors on a single chip with a size of about 1 cm^2 today. Due to the continuous reduction of typical device dimensions, the number of transistors per unit area has increased several orders of magnitude, whereas the cost per chip area has not changed over the last 20 years. This gain in productivity is unique in human history. Technological progress along these lines will certainly continue as long as the cost per function in an IC continues to drop. However, since semiconductor fabrication lines are becoming more and more complex and expensive with each new technological generation, a stop in cost reduction is expected to take place within the next 15 years [4]. This will at least slow down the continuous progress of standard silicon technology. Additionally, physical limitations of conventional technology

become more and more prevailing and will soon strongly contribute to this deceleration of cost reduction. On the long run, these limitations must lead to a replacement of the conventional technology if further technological progress is still required or wanted.

1.1. The metal oxide silicon field effect transistor (MOSFET)

As mentioned, the basis for today's semiconductor devices is the so-called MOSFET, which consists of two highly doped source and drain regions in a silicon substrate with low doping of opposite polarity (see Fig. 1(a)), e.g. p-substrate with n^+-source/drain for an n-channel MOSFET (NMOS). A metallic or poly-silicon top gate insulated from the region between the contacts by a thin insulating film (usually SiO_2) can drive a silicon sheet close to the surface into "strong inversion", resulting (for an NMOS) in the formation of an electron channel between source and drain contact. Above the so-called threshold voltage V_{th}, the transistor becomes conductive for electrons and a drain current I_D begins to flow (for more details see for example Ref. [5]). In Fig. 2 the reduction in gate length as predicted by the Semiconductor Industry Association (SIA)-roadmap is shown. A downscaling far below 100 nm is predicted to be reached in the next few years. Reducing the gate

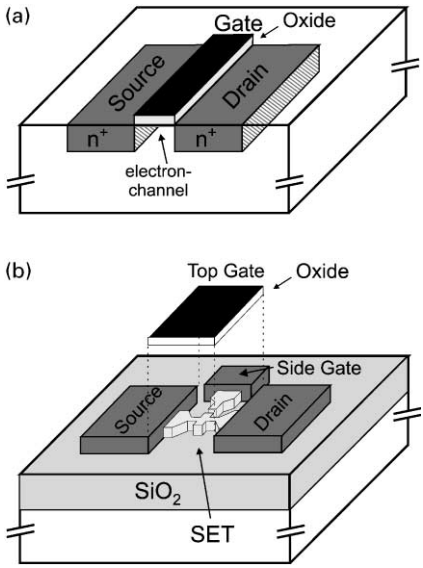

Fig. 1. Comparison of the MOSFET (a) and a silicon-based single-electron transistor (b). Whereas in the conventional MOSFET a conductive electron channel is created between two highly doped source and drain regions by applying a gate voltage to a top electrode, the SET uses the charge quantization in a laterally structured electron island. In contrast to the bulk-MOSFET this kind of SET has to be fabricated out of a silicon-on-insulator film, which provides an intrinsic insulation of the electron island from the substrate.

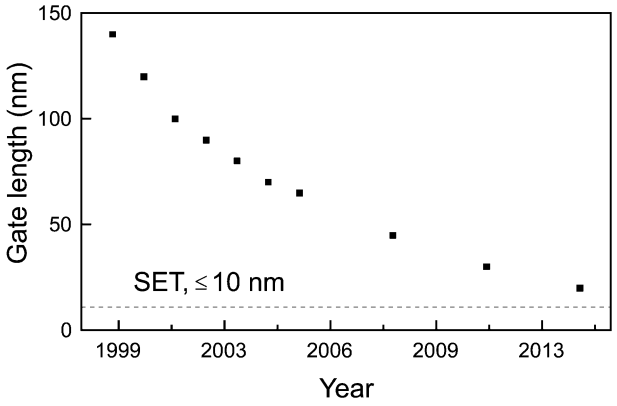

Fig. 2. Predicted gate dimensions following the SIA-roadmap. Minimal structure sizes below 10 nm necessary for reliable SET operation at room temperature are expected to become feasible in about 15–20 years.

length and therefore the source–drain distance can lead to a "punch-through" between source and drain, when the source–drain voltage V_{SD} becomes so large that the depletion regions surrounding source and drain come into close contact. In order to avoid transistor malfunction due to punch-through, the channel region between source and drain has to be doped higher and higher with reduced channel length. To maintain an electric field strength that is still high enough to drive the higher doped silicon into strong inversion without raising the operation voltage, thinner gate oxide films are mandatory. The ultimate limit for SiO_2 as the gate-dielectric is assumed to be 1 nm [6]. Below this limit, direct tunneling from the gate into the substrate becomes too large for proper transistor operation. Although the search for other gate-dielectrics opens up new perspectives for further size-reduction [7], sooner or later this problem will terminate the downscaling of MOSFET. Furthermore, by reducing the device dimensions, dopant fluctuations in the electron channel will become visible which lead to statistical shifts in the threshold voltage V_{th}. An additional problem of scaling the minimum MOS feature size below about 30 nm lies in the increasing "subthreshold current", which is the leakage current between source and drain for a gate voltage $V_G < V_{th}$. This effect is also intrinsic to these MOS devices and causes severe problems in integrating a large number of devices while maintaining low power consumption.

1.2. The single-electron transistor (SET)

Currently, several tentative technologies are investigated in order to overcome the problems arising from scaling device dimensions down to or even below 10 nm. Especially, single-electron devices such as single-electron transistors (SETs) are believed to be able to replace standard MOSFETs in this nanoscale regime. One possible realization of a silicon-based SET embedded in an almost conventional

MOSFET is sketched in Fig. 1(b). A thin silicon-on-insulator (SOI) film (see Section 3) is laterally patterned to form an electron island connected to source and drain by two constrictions. The electron island of the SET can only be charged with electrons at discrete gate voltages (see Section 2 for further details). Therefore, this device can be operated as a switch for electrons based on the quantization of electric charge rather than on the charging of a capacitor like in a MOSFET.

The most outstanding property of SETs is the possibility to switch the device from the insulating to the conducting state by adding only one electron to the gate electrode, whereas a common MOSFET needs about 1000–10,000 electrons (see Section 2). In addition, the switching time of SETs is mainly determined by the *RC*-time constants of the constrictions that can be made very small. Therefore, it is generally assumed that single-electron devices have the potential to be much faster than conventional MOSFETs.

However, one main condition must be satisfied to successfully integrate single-electron devices into standard technology: the devices have to work at room temperature, which requires that their geometrical dimensions be on the order of 10 nm as will be explained in Section 2.

Up to now, several different types of single-electron devices based on SOI or similar structures have been proposed and realized [8–10]. First SETs working at room temperature have already been demonstrated [11,9]. The aim of this review is to present some of these attempts and to compare the physical properties of these devices. Due to its intrinsic similarity, one second type of novel device will also briefly be discussed: an electron waveguide device, a narrow electron channel with a length below the elastic and inelastic electronic mean free path which displays distinct conductance steps as a function of a gate voltage. These steps are caused by the quantization of conductance in one dimension and could also provide the operating principle for room temperature nanometer scale switches.

In Section 2 of this article, a brief introduction to the theoretical framework of single-electron tunneling and conductance quantization is given.

Section 3 focuses on the preparation of SOI-based single-electron structures using high-resolution electron beam lithography.

In Section 4 we introduce the different types of single-electron devices that we realized so far and which are the topic of on-going research. Two major kinds of SOI-based SET-devices are presented: In the first one, a high doping level of the SOI-film in combination with lateral structuring leads to the formation of a serial arrangement of randomly distributed SET-structures in ultrasmall silicon nanowires. When choosing extremely high doping levels (achieved by ion implantation), metal-like Coulomb-blockade (CB) oscillations can be observed in these devices. In a second approach, geometrically defined SET-structures are embedded in the inversion channel of an SOI-MOSFET. These semiconductor "quantum dots" also display CB behaviour. In contrast to the quasi-metallic behaviour of the highly doped devices, the quantum dots show clear quantum signatures resulting from the strong confinement of the electrons on a length scale smaller than the Fermi wavelength λ_F. Similar devices in bulk silicon, where the electron island is defined electrostatically by the so-called split gates are also shown for comparison.

Section 5 deals with our measurements on highly doped SOI-nanowires and also gives a brief overview on results obtained by other research groups.

Section 6 mainly concentrates on quantum dots realized in laterally etched SOI-films. Furthermore, first results on a nanometer-scaled electron waveguide are shown which was also realized in a laterally patterned SOI-MOSFET.

The last Section 7 of this article deals with a novel kind of silicon-based SET-devices: nanomachining of highly doped silicon nanowires or quantum dot structures is used to freely suspend these single-electron structures. Since these suspended devices are thermally decoupled from the underlying semiconductor substrate, phonon–electron interaction mechanisms can be studied.

2. Single-electron tunneling

2.1. Low-dimensional electron systems

The artificial confinement of electrons in a semiconductor structure in one or more spatial dimensions leads to two-, one- or zero-dimensional electron systems [12,13]. When the extensions of a structure in one dimension become of the order of the Fermi wavelength λ_F (the de Broglie-wavelength of the electrons at the Fermi level), quantum-mechanical effects become visible. The electronic density of states is then distributed on discrete subbands with energies E_i. At sufficiently low temperatures the electrons occupy only the lowest subband with energy E_0. This situation characterizes the so-called two-dimensional electron system (2DES). Confining the 2DES in one further dimension leads to a one-dimensional electron channel (1DES) with an electronic density of states

$$D(E) = \frac{g_S g_V}{\pi\hbar} \sum_i \sqrt{\frac{m_{\text{eff}}}{2(E - E_i)}}, \tag{2.1}$$

with g_S and g_V the spin and valley degeneracy and m_{eff} the effective electron mass. In the case where the mean free path of the electrons is much larger than the channel length, electron transport through the wire is ballistic. The current carried by one subband with applied voltage V_{SD} can then be written as

$$I = e \int_{E_F - eV}^{E_F} D(E) v(E)\, \mathrm{d}E = \frac{2e^2}{h} V_{SD} \tag{2.2}$$

with the electron velocity $v(E)$, since

$$D(E)v(E) = D(k) \frac{\mathrm{d}k\, 1\mathrm{d}E}{\mathrm{d}E\hbar\, \mathrm{d}k} = \frac{g_S g_V}{2\pi\hbar}. \tag{2.3}$$

The conductance of one subband is therefore given by

$$G_s = \frac{2e^2}{h} \tag{2.4}$$

with $h = 2\pi\hbar$ Planck's constant. For silicon, where $g_V = 2$, G_s is enhanced to $4e^2/h$. For a ballistic wire, the total conductance is simply the sum over the conductances of

the different subbands

$$G = \sum_{1}^{i} G_s = \frac{2ie^2}{h}. \tag{2.5}$$

This conductance quantization results in a staircase for the I_D/V_{SD} characteristic [14,15] which can possibly be utilized for a novel kind of transistor as sketched in Section 1. Below the first conductance step, where $G < 2e^2/h$, electron transport through such a wire—for short geometries also named quantum point contact (QPC)—is due only to tunneling.

Reducing the last free dimension leads to a 0DES or quantum dot. The spatial quantization of the electron wave function leads to a density of states given by a set of discrete energy levels $\{E_i\}$:

$$D(E) \propto \sum_i \delta(E - E_i). \tag{2.6}$$

2.2. Coulomb blockade oscillations

Electron transport through a quantum dot can only occur, when the dot is coupled to two electron reservoirs, in analogy to conventional MOSFETs termed "source" and "drain". The number of electrons on such an island can only be regarded as fixed when the lifetime broadening $\hbar/\tau$ is much smaller than the Coulomb charging energy

$$E_C = e^2/C. \tag{2.7}$$

Here C denotes the total capacitance of the electron island. Replacing the electronic lifetime τ on the dot by an effective RC-time, the requirement $E_C \gg \hbar/\tau$ can be rewritten as a condition for the coupling strength of the quantum dot to the reservoirs:

$$R \gg h/e^2. \tag{2.8}$$

In order to observe single-electron effects, it is therefore necessary to decouple the quantum dot from the reservoirs via tunneling barriers. Tunneling onto such a quantum dot is normally suppressed by Coulomb repulsion. This "Coulomb blockade" can be lifted, though, if the electrons on the source contact are brought to an energy E_C higher than the electrons in the dot. This can be achieved either by a high source–drain voltage V_{SD} or by changing the dot's potential by a gate voltage V_G with respect to the source potential. Tunneling onto the electron island from the source (drain) can only occur, when the chemical potential $\mu_{S(D)}$ of the reservoir fulfils the condition

$$E(N+1) - E(N) = \mu_{S(D)}, \tag{2.9}$$

where $E(N)$ denotes the total energy of an N-electron system inside the dot [16,17]. The left-hand side of the above equation can be thought of as the discrete chemical potential of the island $\mu_N := E(N+1) - E(N)$. Hence, transport through the

quantum dot can only occur, if

$$\mu_S \geqslant \mu_N \geqslant \mu_D \quad \text{or} \quad \mu_S \leqslant \mu_N \leqslant \mu_D \tag{2.10}$$

At zero bias, when $V_{SD} = (\mu_S - \mu_D)/e = 0$, this condition leads to a series of conductance maxima of the quantum dot whenever V_G aligns the dot's discrete levels μ_N, $\mu_{N+1}\ldots$ with the source and drain chemical potentials $\mu_{S,D}$. In a simple model, one can decompose the N-electron energy $E(N)$ into an electrostatic part and a purely quantum-mechanical contribution, i.e.

$$E(N) = \frac{(Ne)^2}{2C} + \sum_i^N E_i,$$

where the E_i are the single-particle energy levels within the dot [16]. Introducing the single-particle energy level spacing $\delta E_N = E_{N+1} - E_N$, one readily derives an expression for the spacing ΔV_G between two adjacent conductance peaks in the gate characteristic [16]:

$$\Delta V_G = \frac{1}{e}\frac{C}{C_G}\left(\delta E_N + \frac{e^2}{C}\right). \tag{2.11}$$

The conversion factor α links the experimentally accessible conductance peak positions as a function of V_G to the intrinsic energy scale of the quantum dot:

$$\Delta E = \alpha \Delta V_G = e\frac{C_G}{C}\Delta V_G. \tag{2.12}$$

When a small quantum dot is occupied with only a few electrons, the quantum-mechanical contribution δE_N can become significant and strongly alter the periodicity of the Coulomb blockade (CB) oscillations. For silicon dots in the inversion layer of SOI-MOSFETs, δE_N can be comparable to the Coulomb energy and therefore perfect periodicity of the observed conductance peaks cannot be expected.

2.2.1. The single-electron transistor

In the opposite (''metallic'') limit, the electron island is occupied with a large number of electrons [18]. Since λ_F is then much smaller than the size of the island, quantum-mechanical effects are negligible and the term ''quantum dot'' becomes misleading. Transport through such a system is dominated by the Coulomb repulsion of the electrons. For silicon, the metallic limit can be reached in practice by using a very high doping level. Since the conductance peaks are equidistant in this case, switching the electron island from a conducting to a nonconducting state by a proper change of gate voltage can be utilized to operate the device as a ''single-electron transistor'' (SET). In contrast to conventional MOSFETs (as described in Section 1), a change of the island's charge by e just requires one more electron on the gate. This can be easily deduced from a simple capacitor model of the SET where the gate is connected to the electron island via the capacitance C_G.

2.2.2. Nonlinear characteristics

Nonlinear transport characteristics can be obtained, when a voltage difference V_{SD} is applied between the source and drain contacts which is high enough to drive the system out of the linear response regime. In the nonlinear regime, the Coulomb blockade (Fig. 3(a)) can be lifted and several quantum dot levels may contribute to transport. Schematic nonlinear I_D/V_{SD} characteristics are displayed in Fig. 3(d) for the CB case (gap around zero V_{SD}) and for single-electron tunneling (ohmic behaviour), Fig. 3(b). Since a finite difference of the source and drain electrochemical potential allows electrons to flow through the dot as long as an energy level is situated within this "transport window" (Fig. 3(c)), the conductance peaks broaden. A plot of the conductance of the dot against both gate voltage and source–drain bias results in the so-called Coulomb blockade diamond (Fig. 3(e)). The diamond shape reflects the relative positions of source and drain potential and the energy levels within the dot for every combination of the voltage parameters (V_{SD}, V_G). Since the conductance gap in the nonlinear transport characteristic is directly linked to E_C, whereas the spacing between two subsequent conductance peaks is given by $\Delta V_G = e/C_G$, the conversion factor α can be determined by evaluating the slope of the CB-diamond:

$$\alpha = \frac{1e\mathrm{d}V_{G,\diamond}}{2\ \mathrm{d}V_{SD}}. \tag{2.13}$$

Here, $V_{G,\diamond}$ is the gate voltage at the edge of a symmetric diamond as a function of V_{SD}. Eq. (2.13) will be used in Sections 5 and 6 to determine E_C for different SET-devices.

2.2.3. Temperature dependence

The conversion factor α and therefore E_C can alternatively be determined from the temperature dependence of the Coulomb blockade oscillations in the linear regime. The FWHM $\Delta V_{1/2}$ of the conductance peaks varies linearly with temperature [16,19]. In the metallic limit, α is given by the expression

$$\alpha = \frac{5k_B T}{\Delta V_{1/2}} \mathrm{arcosh}\sqrt{2}. \tag{2.14}$$

2.3. Energy scales

Quantum dots based on SOI can be made very small, even down to structure sizes of 10 nm (see Section 3). Simple estimations show that in this regime E_C and δE can almost become of the same order; to obtain a value for the charging energy, we approximate the SET in a very simplified model as a flat metallic disc. The total capacitance of such a conductive disc with radius r embedded in SiO_2 is given by

$$C = 8\varepsilon_r \varepsilon_0 r, \tag{2.15}$$

where ε_r is the dielectric permittivity for SiO_2 and ε_0 the dielectric constant. For a dot with diameter 20 nm this expression together with Eq. (2.7) yields $E_C = 58$ meV. For

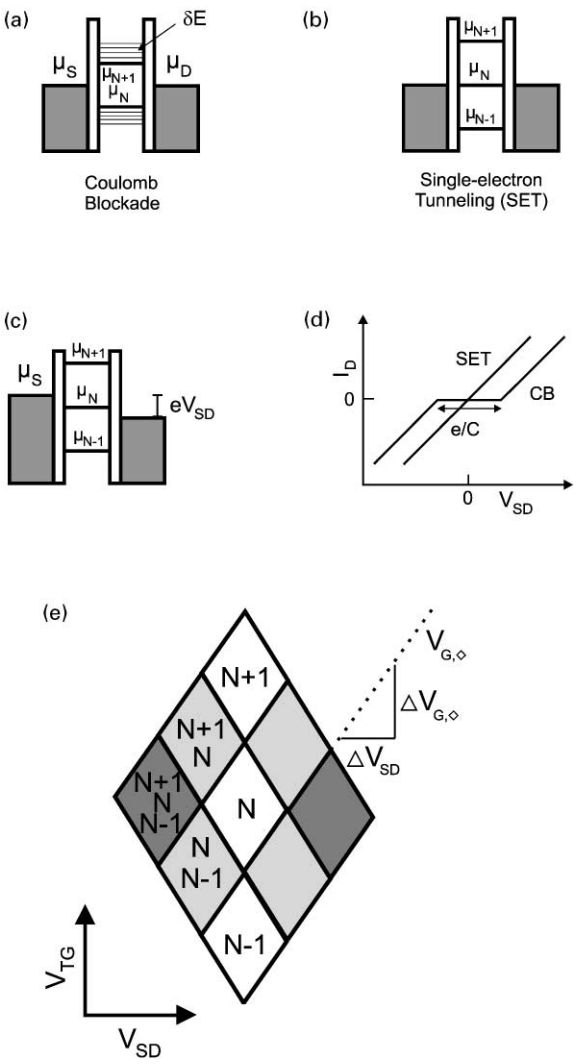

Fig. 3. (a) Coulomb blockade in a single-electron transistor: if the chemical potentials of source and drain leads are not aligned with an energy level inside the electron island, no current can flow through the dot (Coulomb blockade). The energy levels are split in a series of niveaus separated by the single-particle energy δE_N as sketched in (a). Only when the chemical potentials are aligned with one energy level (single-electron tunneling) (b) or if one energy level lies in the gap between the chemical potentials of source and drain (c) current can flow. These two effects lead to the observation of the source-drain characteristic (d) and the CB diamond sketched in (e).

the same SET, the mean quantum mechanical energy level separation $\delta E = (1/g_S g_V)2\hbar^2/m_{\text{eff}} r^2$ is approximately 2–10 meV. This shows that the energy level spacing δE can become comparable to the charging energy in these tiny devices. As a

rule of thumb, Coulomb blockade can be seen until kT is approximately half of E_C. For a reliable room temperature operation of a silicon SET, E_C should therefore be at least $4kT$ and consequently, the dot's diameter should only be around 5–10 nm. In the next Section, preparation techniques to realize such devices will be described.

3. Nanolithography by low-energy electron-beam lithography

The maximum resolution of a lithographic technique depends on both the wavelength of radiation used as well as on the properties of the resist. In semiconductor industry, using advanced optical lithography, presently a resolution down to about 100 nm can be achieved. As mentioned in Section 2, lateral dimensions of about 10 nm or less are necessary in order to define single-electron structures working at room temperature. Today, researchers therefore create lithographically defined nanostructures primarily by electron-beam (e-beam) lithography. Conventional, modestly priced scanning electron microscopes (SEMs) can be easily modified to lithography systems by an external beam control. In this Section we demonstrate, how single-electron devices operating at room temperature can be processed.

3.1. Low-energy electron-beam lithography

In modern SEMs beam diameters and therefore focus spot sizes of down to 1 nm can be realized utilising thermal field emission electron sources. Although the resolution limit using e-beam lithography can therefore be extended to the sub 100 nm regime, fabricating structures with dimensions of about 10 nm is still difficult. Since the resolution limit of electron-beam lithography is primarily set by the properties of the electron resist, novel kinds of high-resolution resists have been investigated. Recently, Fujita et al. [20–22] demonstrated how to use the negative electron resist calixarene to define structures with dimensions of only about 10 nm. However, this resist has to be exposed with high electron doses which leads to severe irradiation damage especially at high electron energies.

One resolution-limiting effect in e-beam lithography is the so-called proximity effect which is caused by scattered electrons in the resist film and by electrons backscattered from the semiconductor substrate. Electrons with energies of tens of keV mainly pass through the resist film and produce low-energy secondary electrons that are partly backscattered from the substrate. Together with the electrons directly scattered in the resist film, these secondary electrons lead to a background exposure of regions in close vicinity of the lithographically defined pattern. Since the penetration depth of electrons is smaller for lower energies, the proximity effect is strongly suppressed in low-energy electron-beam lithography due to the reduction in the number of backscattered electrons from the substrate [23]. For the definition of the nanostructures presented in this article, we used calixarene as a negative e-beam resist. As this resist has a low sensitivity, it is especially important to use low electron

energies. Reducing the electron energy significantly reduces the required electron dose for the exposure, since more electrons are then absorbed in the resist film itself.

In this paragraph we show how we use low-energy electron-beam lithography with calixarene to define single-electron structures down to about 8 nm using a simple single-resist technique. To this end, the exposure parameters of a calixarene resist at electron energies down to 0.5 keV are investigated and the resolution of the resist is determined in the energy range between 1 and 20 keV.

For these experiments, silicon samples were coated with 50 nm thick films of the calixarene resist hexaacetate *p*-methylcalixarene (MC6AOAc). The exposure was performed using a scanning electron microscope with a thermally assisted field-emission electron source and a commercial beam and stage control system.

The relationship between electron energy and required electron dose was determined by exposing patterns consisting of large- and small-scale structures. In addition to that, the specially chosen exposure patterns enabled us to investigate proximity effects occurring at higher electron energies. For a quantitative characterization of our lithography experiments, the following common quantities are determined: Resist contrast γ, minimum gel dose E_G and saturation dose E_1 of the resist. The resist contrast is defined as the absolute value of the measured slope of the resist contrast curve at 50% thickness. The resist contrast curve itself is the experimentally evaluated normalized resist thickness after development as a function of radiation dose, in the present case of the electron dose. Then, for a negative resist, the minimum gel dose is the value of the electron dose, for which a resist film with nonzero thickness still remains on the sample. The saturation dose is the lowest dose, for which the full resist thickness is achieved after development. In the case of large patterns, we determined the saturation dose required for a given resist thickness after exposure. For lower electron doses only a fraction of the resist film remained on the substrate after development [24]. This was confirmed by studies performed with an atomic force microscope (AFM). The step height at the edges of the pattern as well as the slope of the film edge were also determined.

Fig. 4 shows the resist contrast curve for an electron energy of 2 keV. The minimum gel dose is $E_G = 200\ \mu C/cm^2$, the saturation or maximum dose is $E_1 = 800\ \mu C/cm^2$. The contrast γ turns out to be $\gamma = 1.65$, in agreement with the value obtained previously for the exposure of calixarene with 25 keV electrons [23]. Although a value for γ below 2 is commonly regarded as rather poor, the large value of E_G indicates that background exposure by scattered electrons plays no role as long as this background dose does not exceed E_G. This is one reason for the suppression of proximity effects for calixarene, as will be discussed later. The saturation dose E_1, for which the resist film attains its maximum thickness, was determined for different acceleration voltages to obtain the dependence of this dose on the electron energy (Fig. 5). Also shown in Fig. 5 is the required electron dose for narrow lines. Clearly, the electron dose for small structures exceeds the one for large patterns by a factor of about 1.7 over the whole energy range considered. Both plots in Fig. 5 indicate an almost linear relationship between the electron energy and the electron dose.

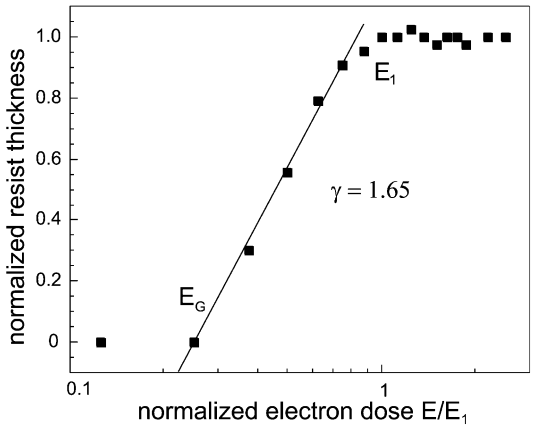

Fig. 4. Resist contrast curve for calixarene exposed with 2 keV electrons. The contrast turns out to be $\gamma = 1.65$.

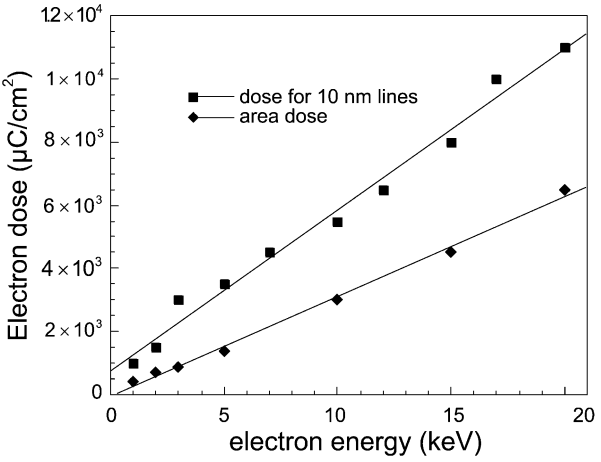

Fig. 5. E_1 as a function of electron energy for narrow lines and for extended areas. E_1 for narrow lines turns out to be about 1.7 times higher than for the large structures.

The slope of the resist edge for different electron doses at an electron energy of 2 keV is shown in Fig. 6. For a dose of 500 $\mu C/cm^2$, just below the saturation dose, the maximum resist thickness is not yet achieved. Increasing the electron dose beyond the saturation dose of 800 $\mu C/cm^2$ to the dose required for the narrow lines of 1500 $\mu C/cm^2$ leads to a steeper resist slope. This shows that structures in the nanometer range can be defined only by using these higher electron doses. The range in which electron scattering is important can be estimated from the width of the resist slope at the saturation dose to be approximately 40 nm. In order to investigate the

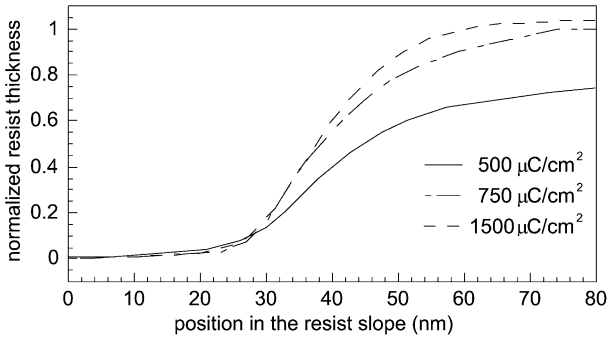

Fig. 6. Resist slope of calixarene exposed with different electron doses at an electron energy of 2 keV. For a dose of 500 $\mu C/cm^2$ below the saturation dose, the maximum resist thickness is not yet achieved.

influence of proximity effects in calixarene, we determined the width of the thin lines in the vicinity of large area patterns in our test structure and found only small broadening due to proximity effects even at the highest electron energy of 20 keV. We therefore conclude that proximity effects play only a minor role in the low-energy regime of electron-beam lithography with calixarene, since the background exposure is smaller than the minimum gel dose E_G. Consequently, calixarene is relatively insensitive to proximity effects. Remarkably, for the lines used in our test structure we found a resolution limit of 10 nm even at accelerating voltages as low as 2 kV. In Fig. 7, an SEM-micrograph of an 8 nm nanowire patterned in a 40 nm thick calixarene film using a 10 keV electron beam is shown.

Summarizing this section, low-energy electron-beam patterning of calixarene in combination with high-resolution thermal-field-emission electron sources provides a lithographic tool that can define resist masks in the nanometer range for subsequent pattern transfer by etching. Though this technology is suitable for research groups, an estimation of the throughput achievable with this serial writing technique demonstrates its practical limitations. With a typical electron dose of 5 mC/cm^2 for calixarene and a beam current of 1 nA (rather high for achieving high resolution) the exposure of an area of only 1% of a typical 1 cm $\times$ 1 cm chip would take a writing time of about 12 h. This example impressively demonstrates that for commercial purposes parallel lithographic techniques are mandatory.

3.2. Outlook

Since novel lithography tools are mandantory for combining maximal resolution in the few 10 nm regime with a high throughput, we give a brief overview of some attempts to develop a sub 100 nm lithography:

The scattering angular limitation projection electron lithography (SCALPEL) [25] technology is a special technique of projection-electron lithography, where electrons pass through a patterned mask similar to conventional optical lithography, and are

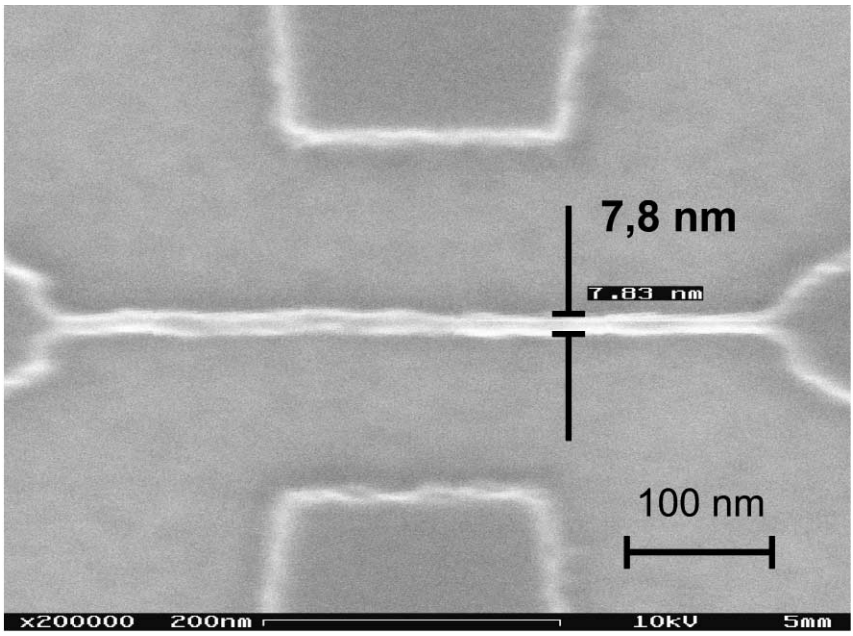

Fig. 7. Scanning electron micrograph of a 8 nm wide nanowire defined in calixarene by low-electron electron-beam lithography.

subsequently focused on the wafer. Therefore, the small de-Broglie wavelength of electrons can be combined with parallel exposure. Another approach to define nanometer sized structures uses the so-called extreme ultraviolet radiation: extreme ultraviolet lithography (EUVL). This technique is more similar to today's ultraviolet lithography and is therefore assumed by many technologists to have the highest potential to overcome the present lithographic limitations. A more comprehensive presentation of most novel lithographic techniques discussed today can be found in [26]. In the near future, the high resolution accomplished by e-beam lithography in today's research labs can probably also be achieved by these novel parallel lithography tools.

3.3. Fabrication technique to prepare single-electron devices in the 10 nm *regime*

The single-electron devices presented in this work are patterned out of silicon-on-insulator (SOI) films which were realized by the separation by implantation of oxygen (SIMOX) technique [27]. These 50 nm thin silicon films are located on 400 nm buried oxide insulating the film from the underlying silicon substrate. In order to investigate different types of SET-devices described in detail in Section 4 the SOI-films used were doped with various donor concentrations. Highly doped source

and drain regions are formed by ion implantation of arsenic through a photoresist protecting the active regions of the silicon film where the SET is patterned afterwards. The silicon film is then thinned to 20–30 nm by thermal oxidation followed by wet etching of the sacrificial oxide in buffered HF. A mesa structure and alignment marks for the subsequent e-beam lithograpic steps are patterned by reactive ion etching (RIE). Next, a 40 nm thick calixarene film is exposed with 10 keV electrons as described in Section 3.1 and this resist-pattern is then transferred into the SOI-film by RIE. In order to achieve a further shrinking of the etched pattern a 5–15 nm thick thermal gate oxide is grown by rapid thermal oxidation. A second, roughly 40 nm thick, layer of silicon oxide is deposited either by sputtering or by plasma enhanced chemical vapour deposition in order to ensure electrical insulation of the SET device. Etching of contact holes at the source and drain regions followed by patterning of a metallic gate and of bonding pads complete the preparation of our devices.

4. Silicon-based single-electron devices

In this section, we briefly present several approaches to the fabrication of reliable room temperature operating silicon-based single-electron devices.

4.1. Split gate technique

The first semiconductor Coulomb blockade devices were realized in high-mobility two-dimensional electron systems (2DES) in $GaAs/Al_xGa_{1-x}As$ heterostructures [28–30]. These 2DES were laterally patterned by Schottky split gates located on top of the heterostructures [31,32]. By electrostatically depleting the 2DES below the split gates a quantum dot structure was formed. For a direct comparison of the findings on the $GaAs/Al_xGa_{1-x}As$ dots with those based on silicon, the split gate realization of an SET-structure can be transferred to conventional field effect transistors [33,34]. In Fig. 8 such a device is depicted. Beneath the metallic top-gate, a split gate is embedded within a thick gate oxide. In contrast to the single-electron devices realized in the $GaAs/Al_xGa_{1-x}As$ system, the 2DES is not depleted by applying a negative voltage to the split gates. Instead, a positive voltage at the top-gate structure leads to the formation of an inversion channel at the silicon/oxide interface, whereas the lower gates locally screen the field of the top-gates. In the regions where the top-gate is screened, inversion is prohibited and the 2DES is patterned in the shape of a quantum dot. In Fig. 9 the conductance $g = dI_D/dV_{SD}$ of such a silicon quantum dot as a function of the top-gate voltage V_{TG} is shown. The measurement was performed in a dilution refrigerator at a temperature of $T = 50$ mK. Distinct Coulomb blockade oscillations are visible similar to those observed in $GaAs/Al_xGa_{1-x}As$ dots [30]. The good periodicity of the conductance oscillations show that the quantum mechanical single-particle energy δE is much smaller than the Coulomb charging energy E_C (cf. Eq. (2.11)). The Coulomb charging energy can be determined by recording the Coulomb blockade diamond

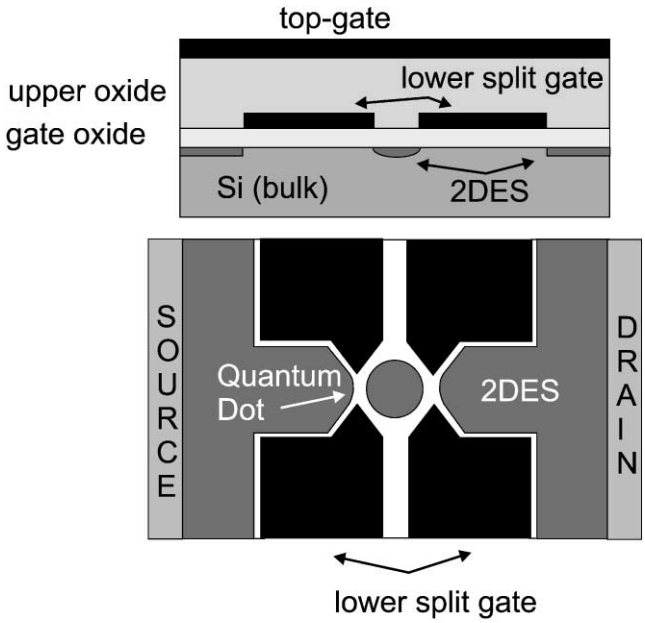

Fig. 8. Silicon quantum dot realized in bulk silicon by a dual gate technique. The positively biased metallic top-gate leads to the formation of a 2DES at the silicon/oxide interface. The split gates screen the electric fields provided by the top-gate and thus pattern the 2DES electrostatically.

described in Section 2. Using Eq. (2.13), E_C can be deduced from the peak-to-peak spacing. This yields $E_C \approx 2$ meV for the entire gate voltage range investigated. Due to the small value of E_C the conductance oscillations are visible only up to temperatures of about $T \approx 10$ K. As a matter of principle, since the electrostatic field spreads out in the insulating gate oxide between the active silicon area and the split gate, the lateral extensions of these devices cannot be scaled down to the 10 nm regime. In order to fabricate single-electron devices with smaller dimensions, lateral patterning of the active silicon must be accomplished by etching. As discussed in Section 1, SOI has to be used for that purpose. Using the preparation technique described in Section 3, we fabricated various SOI-SETs which are presented in the next sections. These devices can be distinguished by their doping level. Similar to conventional MOSFETs, the electron channel can be conductive even at zero gate voltage (depletion MOSFET) or can be made conductive by applying a positive gate voltage resulting in an inversion channel at the Si/SiO_2-interface [5]. Depletion MOSFETs are obtained by doping the channel region with donors such as arsenic or phosphorous. In contrast to MOSFETs, doping of SET-structures fundamentally alters the electronic properties of these devices. For SET devices, the mean distance between donors can become of the same order as the dimensions of the structure. Doping fluctuations in highly *n*-doped silicon SET-structures result in strong local potential variations, as will be discussed in the next section.

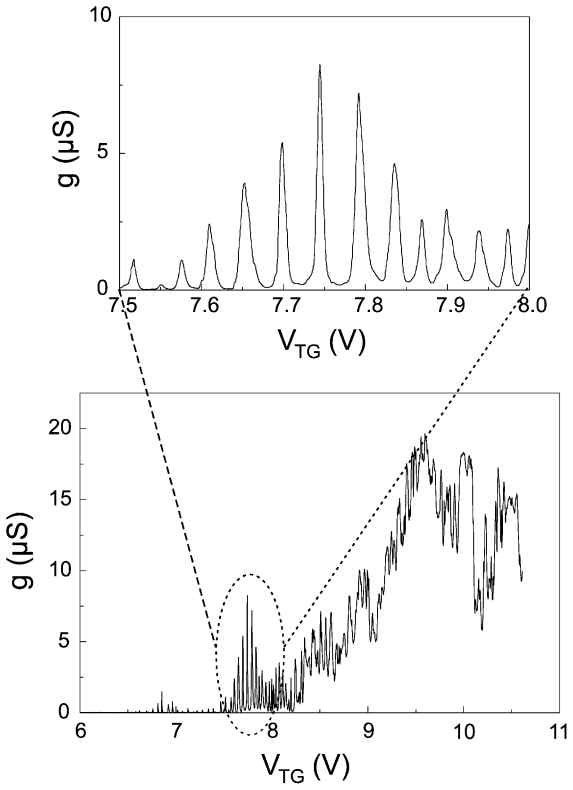

Fig. 9. Coulomb blockade oscillations of a bulk-silicon quantum dot. The charging energy is estimated to be $E_C \approx 2$ meV.

4.2. Highly doped silicon nanowires

In order to investigate the electrical behaviour of highly *n*-doped SOI-nanostructures we fabricated tiny nanowires in the 10 nm regime. Smith and Ahmed fabricated similar conducting silicon SOI-wires with lateral dimensions down to about 40 nm using highly doped SOI material [10]. In this reference, it was possible to resolve conductance oscillations upon changing a control gate voltage. The control gate was realized as an in-plane side-gate within the highly doped SOI film. Although the mean peak-to-peak spacing was constant in subsequent gate sweeps, both the exact peak positions as well as the peak amplitudes differed. This observation can be interpreted in terms of the formation of randomly distributed electron islands separated by tunneling barriers formed by dopant fluctuations within the nanostructure. Fig. 10 illustrates the formation of a single-electron structure in these nanowires. In a one-dimensional picture the edge of the conduction band E_C varies due to the local variation of the doping level along the wire. At zero gate voltage (and zero temperature) the wire is conductive and the chemical potential

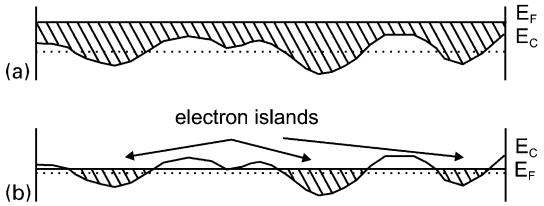

Fig. 10. Schematic drawing of the potential fluctuations along a highly doped SOI-nanowire. In (a) the highly conducting wire has a chemical potential E_F high above the fluctuating edge of the conductance band E_C. When the wire is depleted, isolated electrons islands appear, leading to a serial arrangement of SETs.

E_F is far above E_C (Fig. 10(a)). If the electron density is lowered by the application of a gate voltage negative with respect to the wire, E_F can partially become lower than E_C as depicted in Fig. 10(b). When this "percolation level" is crossed, isolated electron islands are formed. Usually, a serial arrangement of SETs is formed, and therefore these structures do not display conductance peaks with an exact periodicity.

4.3. Silicon-on-insulator quantum dots

In highly doped silicon nanowires electron islands are formed by local variations of the internal electrostatic potential. Quantum dot structures in highly doped SOI films can also be realized intentionally by lithographic definition [35]. These devices show Coulomb blockade oscillations in an intermediate depletion regime. On the one hand, depletion must be strong enough to let the narrow constrictions of the quantum dot structure act as tunneling barriers. At the same time, the quantum dot should not disintegrate into small electron islands due to dopant fluctuations, which happens for stronger depletion. Although in the measurements in Ref. [35] on SOI-SETs clear conductance oscillations can be observed, a difficult tuning procedure of these SETs with the silicon substrate as an intrinsic back-gate is necessary to find a proper working point. However, the use of undoped (or weakly *p*-doped) SOI films in the regions where the SET is embedded into the inversion channel of a MOSFET circumvents the awkward influence of doping fluctuations. Such devices were the first to allow the observation of CB oscillations up to very high temperatures [8]. Since the tunneling barriers are defined by the geometry of the electron channel, the tunability of these devices is greatly enhanced in comparison with the rather random effects found in highly doped nanowires. By application of a top-gate voltage, the conductance of the barriers can easily be adjusted to fulfil Eq. (2.8). On the other hand, the strong influence of the quantum mechanical level separation in these semiconductor quantum dots makes an application for single electronics more difficult as in the case of quasi-metallic devices. According to Eq. (2.11) the periodicity of the classical CB is lifted by the influence of discrete energy levels inside a semiconductor quantum dot in the 10 nm range.

Although first successful measurements on this kind of devices were made on geometrically defined structures [8], randomly formed single-electron structures were observed recently in SOI-nanowires [11] and SOI-quantum point contacts [9]. The formation of a serial arrangement of electron islands inside a nanowire can easily be understood in terms of edge-roughness during the fabrication process. Although many efforts were made recently to investigate the origin of SET-formation in SOI-quantum point contacts [36], until now the underlying mechanism remains unclear.

In the next section we present our measurements on most of the SOI-SETs described above. We compare the experimental results primarily with regard to high-temperature operation. Finally, we show measurements on SOI-quantum wires acting as electron waveguides. Apart from Coulomb blockade devices, these novel electronic switches are also regarded as promising candidates for a future technology replacing MOSFETs (cf. Section 1).

5. Highly doped SOI-nanostructures

In the following section we present electron transport measurements on various highly doped silicon nanowires. These wires differ both in geometry and in their doping level. As will be shown, the electronic properties of these wires depend crucially on these two parameters. The temperature-dependent conductance of these silicon wires as well as of the SET structures treated in the following sections were measured in a ^{4}He-bath cryostat with a variable temperature insert, allowing continuous operation in the temperature range 1.5–200 K. The conductance was measured with a standard lock-in technique, typically operating at a frequency of 130 Hz.

5.1. Highly doped silicon nanowires in a dual-gate configuration

In contrast to the common side-gate configuration used in earlier publications [10], our nanowire devices contain both one side-gate and a metallic top-gate. The electrical potential inside the highly doped wire can be tuned independently by variation of the top- and the side-gate voltages V_{TG} and V_{SG}.

A schematic cross-section drawing of this structure with the symbols used in the text is shown in Fig. 11. The wire was patterned out of a 50 nm thin SIMOX film in which a high concentration of arsenic was implanted. The implantation dose was 6.3×10^{14} cm^{-2} at an energy of 20 keV, leading to a nominal doping level of about $N_D \approx 10^{20}$ cm^{-3}.

In Fig. 12, the conductance $g = dI_D/dV_{SD}$ of a silicon wire with width $w \approx 10$ nm and thickness $h \approx 25$ nm (these values result from shrinking by thermal oxidation) is plotted versus the depleting top-gate voltage V_{TG} at a temperature of $T = 2$ K. The dimensions of the wire are similar to those in Ref. [10]. A large number of quasi-periodic conductance oscillations are observed, which can be attributed to single-electron charging effects.

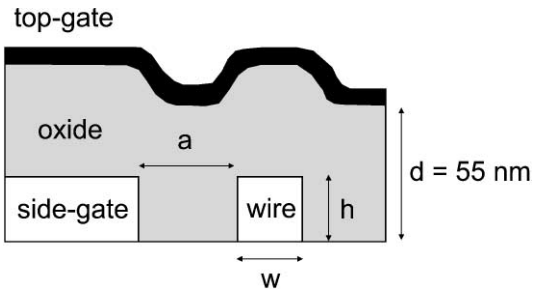

Fig. 11. Sketch of the device: The in-plane side-gate is located at a distance $a = 95$ nm from the silicon nanowire, which has a width w of about 10 nm and a length of $l = 500$ nm. The silicon film thickness is estimated to be about $h = 25$ nm. Both structures are embedded into SiO_2, which serves as gate-oxide with a thickness of $d = 55$ nm. On top, a metallic gate is located, controlling the electrical potential in both the nanowire and the side-gate.

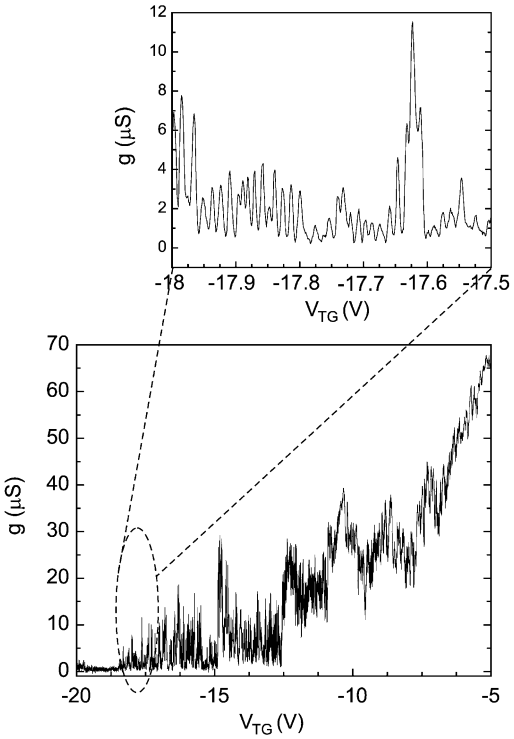

Fig. 12. Single-electron effects in a highly doped, 10 nm wide silicon wire at $T = 2$ K as a function of the top-gate voltage V_{TG}. Almost periodic conductance oscillations can be found. However, both the peak amplitudes as well as the exact peak positions differ between subsequent gate sweeps.

The patterning of nanometer size top-gate structures atop an embedded SET is not possible with today's lithography with sufficient overlay accuracy. Also with the SEM-tool we used, this is a challenging venture. Therefore, individual control of

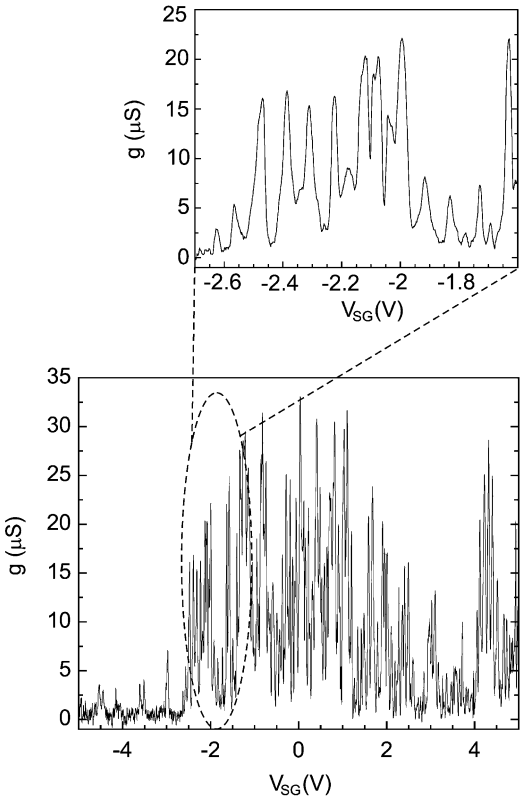

Fig. 13. Controlling the electrostatic potential of the wire via an in-plane side-gate causes conductance oscillations. The mean period of these oscillations differs from that observed in Fig. 12. The top-gate voltage in this measurement is $V_{TG} = 17.5$ V, which allows low side-gate voltages to control the CB oscillations.

different SET-devices is possible only by utilising laterally defined side-gates which can be patterned simultaneously with the nanowire in one single lithographic process. In addition, when the top-gate voltage is kept constant, a variable side-gate voltage can independently control the conductance oscillations. As an example, in Fig. 13 the top-gate voltage is set to a value near pinch-off. Changing the side-gate voltage V_{SG} results in conductance oscillations resembling those of Fig. 12. This allows to minimize the controlling side-gate voltage which is of special importance for possible applications of these devices within integrated circuits.

5.1.1. Temperature dependence

In order to derive the Coulomb charging energy E_C of the nanowire according to Eq. (2.13), the determination of the conversion factor α is necessary. As reported similarly by Smith and Ahmed [10], the conductance oscillations of the nanowire

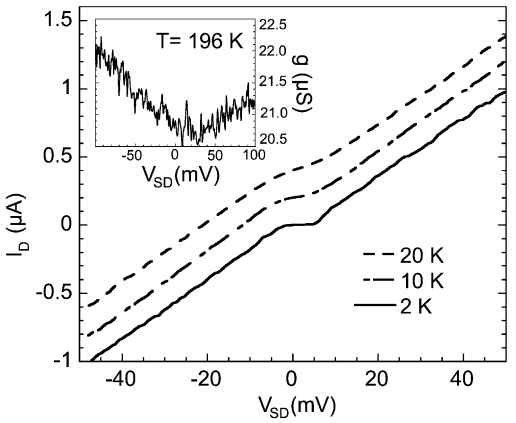

Fig. 14. Temperature dependence of the I_D/V_{TG} trace. The wire shows a distinct nonohmic behaviour at temperatures up to 20 K. Single-electron effects remain visible only weakly up to temperatures of about 200 K (see inset).

were not stable in time and we therefore were not able to record a Coulomb blockade diamond. Instead, we used a conversion factor $\alpha_{TG} \approx 50$ meV/V observed in similar structures which will be described later. With this value, we obtain $E_C \approx 0.7$ meV, which seems to be too small to be interpreted as the charging energy of a single-electron island with lateral dimensions below 20 nm. Also the temperature dependence of the nonlinear source–drain characteristic shown in Fig. 14 and of the gate-characteristic (not shown here) clearly contradict a charging energy below 1 meV. Interpreting the observed conductance oscillations in terms of Coulomb blockade through multiple tunnel junctions (MTJ), single-electron effects should remain visible up to very high temperatures due to the small size of the nanowire. However, in Fig. 14 only a weak nonlinearity can be observed at temperatures up to 200 K. We therefore conclude that the tunnel barriers formed by random dopant distribution must be very shallow, so that the condition Eq. (2.8) cannot be met at higher temperatures. Remarkably, although many efforts were recently made to use highly doped SOI-films for single electronics with structure sizes in the same range as reported here, no high-temperature operation (i.e. 300 K) of these devices has been observed yet [10,37–39].

If one assumes the statistical dopant fluctuations to be proportional to $\sqrt{N_D}$ (with N_D the donor concentration) [40], the random fluctuations should be on the order of 10 donors per 10 nm^3 for $N_D = 10^{20}$ cm^{-3}. Since both common *n*-dopants for silicon, As and P, pile up during dry oxidation with a segregation coefficient of about 10 [41], also the dopant fluctuations due to segregation effects have to be taken into account in the process of MTJ-formation.

5.1.2. Side-gate versus top-gate

The conversion factor α differs for the top-gate and for the side-gate. Variation of the corresponding gate voltages therefore results in conductance oscillations of

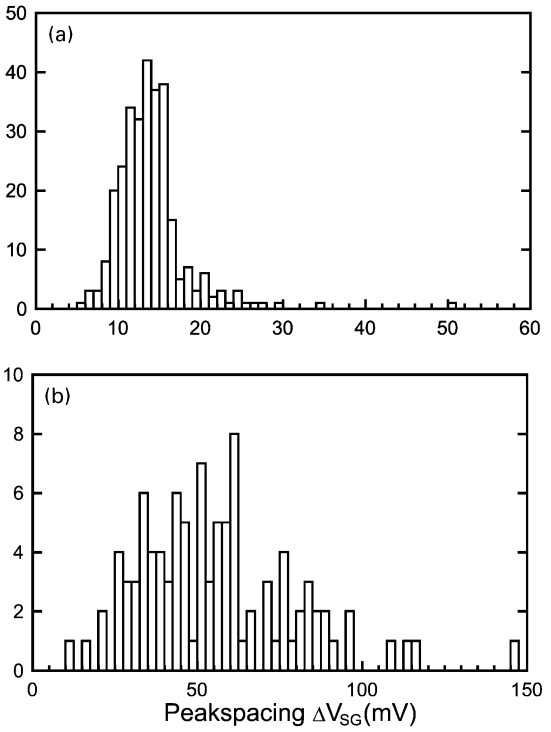

Fig. 15. Distribution for the peak-to-peak spacings found in Figs. 12 and 13. The histogram in (a) shows the distribution for V_{TG}, in (b) the curve for V_{SG} is shown. The curve in (b) clearly shows a larger broadening than the plot in (a). The normalized standard deviation for the distribution in (a) is $\sigma_{TG} = 0.32$ and in (b) $\sigma_{SG} = 0.43$.

different periodicity. However, the periodicity of the oscillations as a function of the side-gate voltage V_{SG} seems to be not as good as for the top-gate voltage. In Fig. 15 we compare the distribution of the peak spacings ΔV_{TG} and ΔV_{SG}. Fig. 15(a) shows the distribution for ΔV_{TG} and Fig. 15(b) the distribution for ΔV_{SG}. Obviously, the distribution of the peak spacing is broader when the oscillations are controlled via the side-gate. Consequently, the normalized standard deviation $\sigma = \sqrt{\langle(1 - \Delta V/\langle\Delta V\rangle)^2\rangle}$ for the distribution in Fig. 15(b) $\sigma_{SG} = 0.43$ is larger than $\sigma_{TG} = 0.32$ in Fig. 15(a). Formation of MTJ inside the silicon nanowire by the application of a negative top-gate voltage also depletes the silicon side-gate. Since the dimensions of the side-gate are on the order of 100 nm, it is reasonable to assume the formation of strong potential fluctuations inside this highly doped silicon structure. These potential fluctuations are also altered by V_{SG}, since a variation of this voltage simultaneously changes the voltage between side-gate and top-gate. Presumably, these fluctuations in the potential landscape of the side electrode are responsible for the stronger variation of the peak-to-peak spacing when the conductance is controlled by V_{SG} rather than by V_{TG}.

In order to achieve a better understanding of these dual gate structures, we compare the capacitances between the electron island formed in the silicon nanowire by random dopant fluctuation and the top- and side-gate, respectively. The ratio between these capacitances can easily be determined by comparing the mean peak-to-peak spacing in Figs. 12 and 13. Since the total capacitance of the wire C can be written both in terms of C_{TG} and of C_{SG} using the conversion factors α defined in Eq. (2.13)

$$C = \frac{e}{\alpha_{TG}} \cdot C_{TG} = \frac{e}{\alpha_{SG}} \cdot C_{SG}, \tag{5.1}$$

one can derive the ratio of C_{TG} and C_{SG} to $C_{SG}/C_{TG} = \Delta V_{TG}/\Delta V_{SG} \approx 0.25$.

Approximating C_{TG} by a simple plate capacitor with an area $A = w \times l$ leads to $C_{TG} \approx 3.5$ aF. In our devices, the distance a between the in-plane side-gate and the silicon wire is larger than the wire width. For a rough estimate, we therefore use a formula for the in-plane capacitance of an infinite thin wire in front of an infinite side-gate with $w \ll a$ [42]:

$$C_{SG} \approx \frac{\varepsilon_0 \varepsilon_r \pi}{\ln(4a/w)} \cdot l \tag{5.2}$$

and find $C_{SG} \approx 6$ aF. In Eq. (5.2), ε_r is the dielectric permittivity of SiO_2 and ε_0 the dielectric constant of free space. In these approximations the ratio of the two capacitances is estimated to be $C_{SG}/C_{TG} \approx 1.7$. Including stray-fields in a more sophisticated model leads to a reduced value of $C_{SG}/C_{TG} \approx 1.2$. Nevertheless, despite the crude assumptions underlying this estimation, the side-gate capacitance seems to be too small in comparison to the top-gate capacitance.

5.2. Quasi-metallic Coulomb blockade in silicon nanowires

We also fabricated silicon nanowires from SOI-films with even higher doping. The measurements described in this section were performed on nanowires patterned out of SIMOX films implanted with arsenic ions with a dose of 2×10^{15} cm^{-2} at an energy of 20 keV. This led to a mean dopant concentration of $N_D \approx 4 \times 10^{20}$ cm^{-3} with an implantation peak of about 10^{21} cm^{-3}. In Hall-measurements on larger structures we found that about 50% of the implanted donors were electrically active at a temperature of 4 K.

The mean distance between the dopants is only 2 nm and for an unprocessed wafer the distribution of dopant atoms can be assumed to be rather uniform. The electron number in an ideal dot with extensions of about 50 nm fabricated from this material is on the order of 10^5.

Fig. 16(a) depicts the conductance of a 50 nm wide and 30 nm thick nanowire at a temperature of 4.2 K as a function of the applied top-gate voltage. Oscillations with a clear periodicity are observed, indicating the metallic nature of the SET. On the other hand, the high offset in the valleys of the conductance indicates a highly conductive parallel channel. Fig. 16(b) shows a contour plot of the channel conductance versus top-gate voltage V_{TG} and source–drain bias V_{SD}. From the slope of the edges of this Coulomb blockade diamond we determine the charging

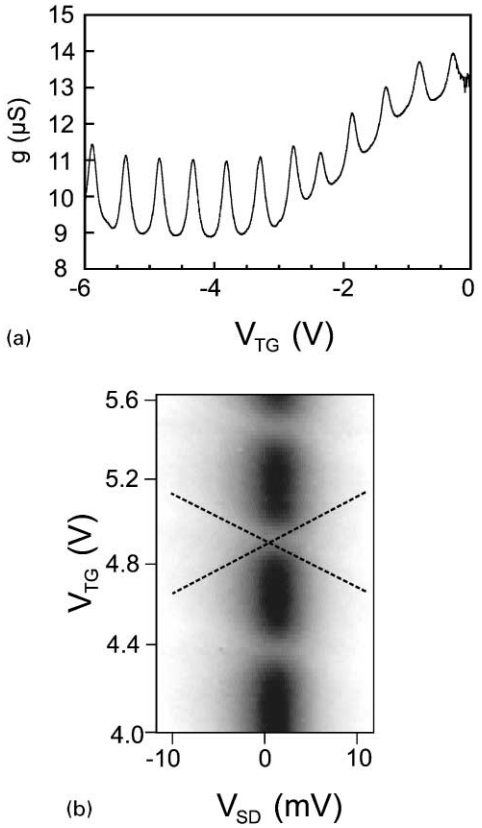

Fig. 16. (a) CB oscillations in a quasi-metallic nanowire showing almost perfect periodicity. (b) CB diamond for the structure measured in (a). From the slope of the diamond the charging energy of the dot formed inside the wire can be estimated.

energy separation in the SET using Eq. (2.13) and obtain $\alpha = 0.033$ eV/V and $E_C = 17.5$ meV. This corresponds to a total capacitance of $C = 10$ aF. In the approximation of an island in the shape of a flat cylinder, the diameter of the SET can be estimated to be about 70 nm. Presumably, the real island is more extended along the wire than perpendicular to it. Therefore, this value is in good agreement with the lithographic dimension of the wire.

In Fig. 17 the temperature dependence of the conductance is presented. The oscillations remain visible up to temperatures above 70 K. Since CB should persist until the thermal energy $k_B T$ exceeds half of the charging energy $E_C = e^2/C$, this result also suggests a charging energy of about 15 meV. However, from a fit of the shape of the conductance peaks in Fig. 17 according to Eq. (2.14), a conversion factor $\alpha = 0.12$ eV/V and a charging energy $E_C = 63$ meV is obtained. These values differ strongly from those derived from the CB diamond. We believe that this deviation is due to the presence of a conductive parallel channel in the nanowire,

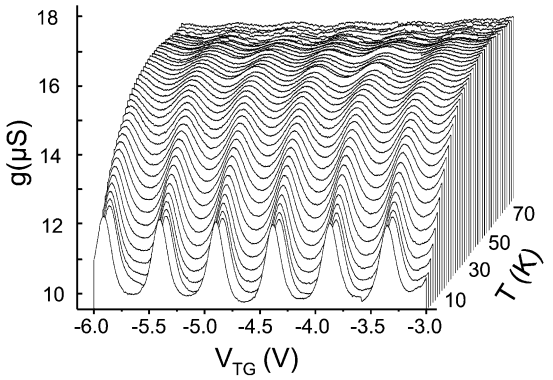

Fig. 17. Temperature dependence of the CB oscillations shown in Fig. 16(a). The oscillations remain visible up to temperatures of almost 100 K.

whose conductance strongly alters the shape of the conductance peaks caused by the SET alone [43]. As the doping level of the material is extremely high, it is not reasonable to assume that random dopant fluctuations are able to form single-electron islands inside the nanowires. Presumably, the pattern dependent two-dimensional oxidation of laterally structured SOI-devices in combination with the pile-up effect of As-dopants during dry oxidation leads to the observed SET-structure. In fact, since the thermal oxidation of nanometer scale curved structures is extremely sensitive to the geometry, in particular to the radius of curvature, the oxidation rate can vary significantly along a Si-nanowire with some edge roughness [44]. Additionally, the formation of SiAs precipitates has been observed under similar conditions [45]. Our observation of a relatively high parallel conductance can also be explained in this picture, suggesting the formation of an isolated electron island inside the wire, whereas the rest of a wire remains ohmic.

Although we achieved the formation of single metallic islands in the nanowire discussed above, we also observed the formation of serial arrangements of metallic electron islands in other devices. In this case, the devices show nonperiodic conductance oscillations and also an obvious response to a magnetic field applied perpendicularly to the wire, as shown in Fig. 18. We believe that the tunneling barriers formed randomly inside the nanowires by segregation effects are strongly affected by a magnetic field, which is in stark contrast to the hard potential wall formed at the Si/SiO_2 interface as will be shown in Section 6.

In conclusion, the use of both highly doped nanowires as well as of quasi-metallic silicon nanowires allows for the observation of single-electron effects up to temperatures of about 100 K. Quasi-metallic structures allow the observation of almost perfect Coulomb blockade. Nevertheless, both devices suffer either from poor reproducibility of their electrical properties or from a high parallel conductance inside the wires since it is not possible to deplete these extremely doped structures near pinch-off.

In contrast to recent work by Single et al. [35], we did not succeed in fabricating highly doped dot structures showing Coulomb blockade oscillations. Due to the

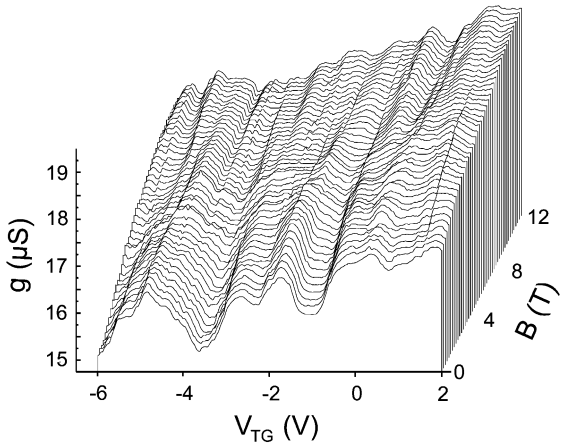

Fig. 18. CB oscillations in a quasi-metallic nanowire. No periodicity is revealed, indicating the formation of a serial arrangement of metallic islands. Although the conductance oscillations are almost unaffected by a magnetic field—indicating a hard potential wall—the tunnel junctions between adjacent electron islands in the serial arrangement show a strong influence of the magnetic field.

higher doping level in our SIMOX-films, the geometrically defined tunneling barriers had too high a conductance to meet the tunneling barrier condition of Eq. (2.8). Moreover, since multiple tunnel junctions spontaneously form in almost every doped nanostructure we investigated, a clear distinction between MTJ and dot-geometry is hard to make [39]. Therefore, we favour quantum dots embedded in inversion MOSFETs as the better candidates for reliable high-temperature operating single-electron devices. These devices will be described in the next Section 6.

6. Single-electron tunneling in silicon quantum dots

In the devices described in this section, electrons were confined in the inversion layer of an SOI-MOSFET by lateral patterning of the SOI-film (Fig. 1(b)). We investigated the electronic transport properties of various such devices with different geometries. The *p*-doping level of our SOI substrates is so low that on the average no dopant is located in a quantum dot with dimensions of about $20 \times 20 \times 20\ \mathrm{nm}^3$. Therefore, random dopant fluctuations can be ruled out in these devices. Moreover, since the conductance of the constrictions terminating the dot structure can easily be controlled by the gate voltage and varied in a wide range, the Coulomb blockade oscillations observed become fairly reproducible.

6.1. Coulomb blockade oscillations

In Fig. 19, CB conductance oscillations of a quantum dot (dot♯1) with lithographical diameter of 20 nm are shown. Although the conductance peaks are

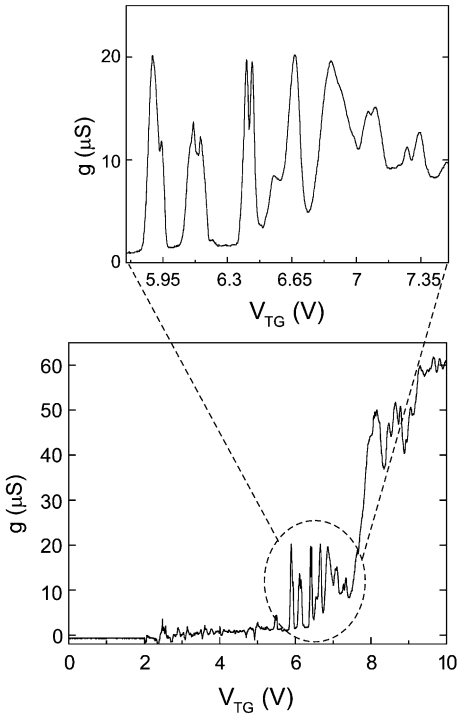

Fig. 19. Coulomb blockade oscillations in a 20 nm inversion quantum dot at a temperature of 2 K.

almost equidistant at $V_{TG} > 6$ V a slight deviation from the classical periodicity of the oscillations is observed, as can also be seen in the distorted CB diamond in Fig. 21(a). This presumably indicates influences of energy quantization within the dot. From the slope of the diamond and the mean spacing between two adjacent conductance oscillations one can deduce the conversion factor $\alpha = 0.101$ eV/V, the charging energy $E_C = 56$ meV and, assuming a disc shape for the dot and using Eq. (2.13), a geometrical dot diameter of $d = 22$ nm. In Fig. 20 the Coulomb blockade oscillations of a somewhat larger dot (dot#2) is shown. For this dot the most pronounced conductance oscillations are visible at higher gate voltages than for the smaller dot. The above-mentioned calculations now yield $\alpha = 0.154$ eV/V, $E_C = 41$ meV and $d = 30$ nm. Therefore, we can assume that the number of electrons inside this dot is larger, which results in a more metallic behaviour. Consequently, the peak spacings become more uniform and the Coulomb blockade diamond in Fig. 21(b) much less distorted than in Fig. 21(a). In order to investigate the properties of the confining potential at the Si–SiO_2 interface, we measured both the gate characteristic as well as the nonlinear source–drain characteristic as a function of the magnetic field applied perpendicularly to the transport direction. The influence of a magnetic field on the energy levels of a quantum dot can be understood within a simple model system: the energy eigenvalues of a two-dimensional harmonic

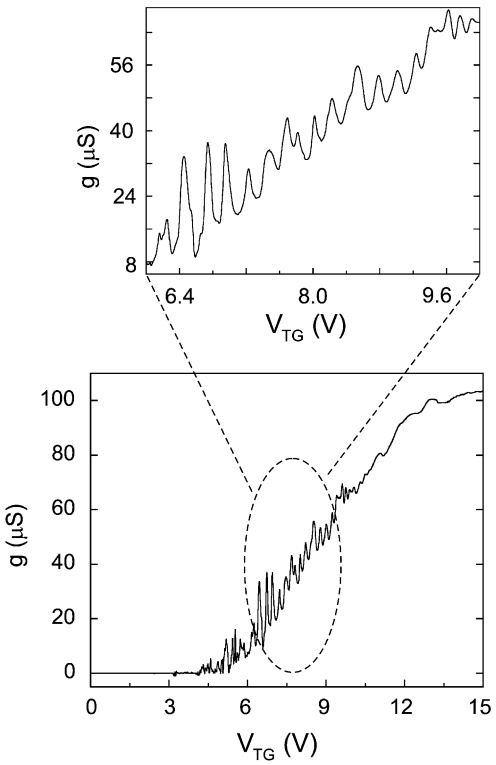

Fig. 20. Coulomb blockade oscillations in a 25 nm inversion quantum dot at a temperature of 2 K. In comparison to Fig. 19 the oscillations display a better periodicity with V_{TG}.

potential with angular frequency ω_0 are altered by a perpendicular magnetic field as [46,47]

$$E_{nl} = (2n + |l| + 1)\hbar\omega_{\text{eff}} + l\hbar\omega_c/2. \tag{6.1}$$

Here, $\omega_{\text{eff}} = \sqrt{\omega_0^2 + \omega_c^2/4}$ with $\omega_c = eB/m_{\text{eff}}$ the cyclotron frequency and m_{eff} the effective electron mass of silicon in the (100)-direction. We therefore only expect the quantum-mechanical level spacing to be altered in a magnetic field, if the confining potential is weak and ω_0 of the order of ω_c. In Figs. 22(a) and (b) the magnetic field dependence of the gate-characteristic and the nonlinear characteristic of dot♯1 are shown, respectively. Obviously, in both measurements no significant influence of the magnetic field on the electronic properties of the quantum dot can be observed.

The spacing between the first and the second conductance peak is considerably larger than the mean peak spacing at higher V_{TG} indicating a relatively large influence of the quantum-mechanical level spacing. Especially, the spacing between the first and the second peak does not depend on the magnetic field. It can therefore be assumed that the effective potential in the dot is not altered significantly and electrons are therefore confined within a hard-wall potential.

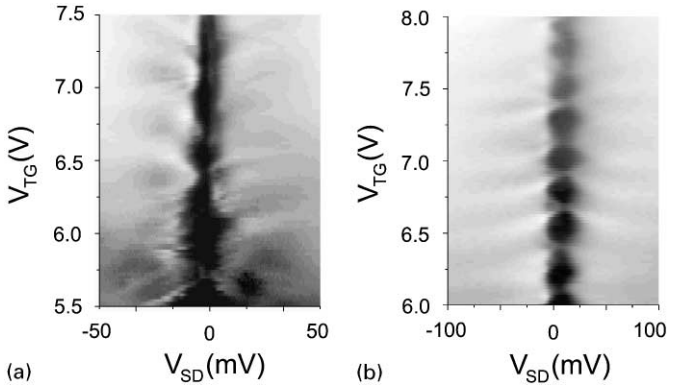

Fig. 21. Grey-scale plots of the channel differential conductances versus top-gate voltage V_{TG} and source/drain bias V_{SD} of both quantum dots are shown. From the slope of the Coulomb blockade diamonds one can determine the energy level separations. The plot in (a) (dot#1) diplays a rich fine structure at nonzero bias, whereas the Coulomb blockade diamond in (b) (dot#2) almost shows a metallic behaviour.

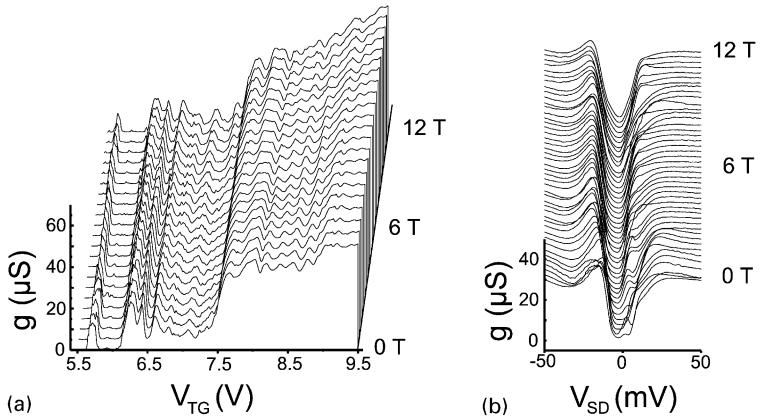

Fig. 22. Magnetic field dependence of the Coulomb blockade oscillations (a) and of the nonlinear characterisic (b) at $T = 2$ K. No significant influence of the magnetic field can be observed.

6.2. Temperature dependence

In Fig. 23 the temperature dependence of the gate characteristic is shown. Clear CB oscillations up to temperatures above 100 K are visible. The first conductance maximum displays almost no change in shape in the temperature range between 2 and 100 K, whereas the subsequent oscillations at higher top-gate voltages V_{TG} clearly begin to smear out towards higher temperatures. In greater detail, we examined the temperature dependence of the nonlinear characteristic of the smaller

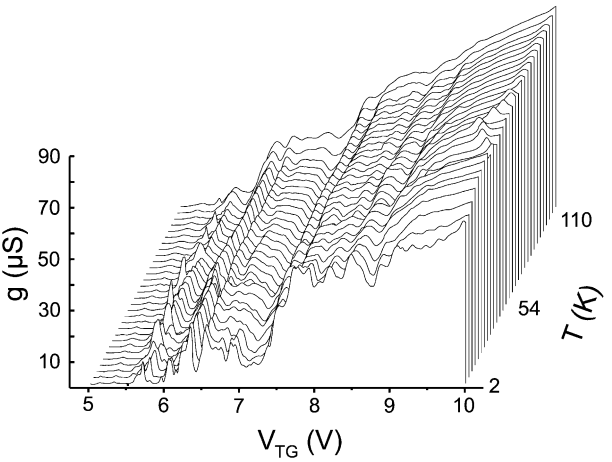

Fig. 23. Temperature dependence of the conductance oscillations of the 20 nm dot. Especially, the first conductance maximum is almost unaffected by the temperature rise up to 110 K.

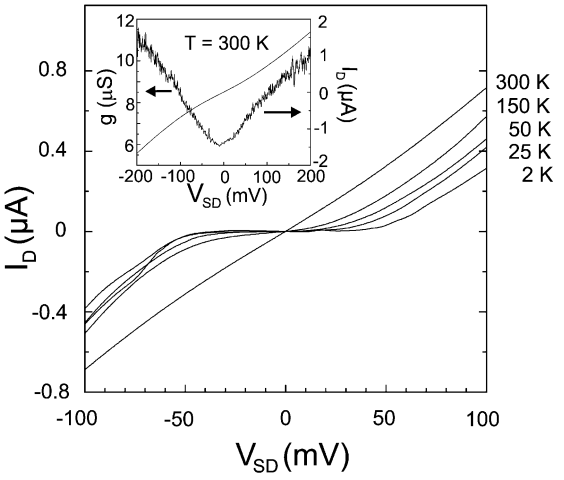

Fig. 24. Temperature dependence of the nonlinear characteristic. At $T = 300$ K a distinct Coulomb blockade gap remains visible.

dot (Figs. 19 and 21(a)) in the conductance valley adjacent to the first conductance maximum (Fig. 24). A clear CB gap in the conductance is found even at room temperature. Since in this device CB should remain visible up to temperatures of $T = E_C/(2k_B) \approx 310$ K, this finding is in good agreement with the theoretical expectations.

6.3. Quantum wires

In order to prove that our SET-structures were indeed defined lithographically, we prepared SOI-nanowires embedded in SOI-inversion MOSFETs with various widths and lengths. In none of these nanowires CB oscillations could be resolved. In Fig. 25(a) the conductance of a 25 nm wide nanowire is shown. Since we do not shrink our nanostructures by thermal oxidation as strongly as in Ref. [11], width fluctuations obviously do not lead to an accidental formation of electron islands. Therefore, our fabrication method is expected to be highly reproducible even at structure sizes in the 10 nm regime. We did not observe a Coulomb blockade diamond in this structure as can be judged from the nonlinear I_D/V_{SD}-characteristics. Consequently, the features observed in the gate characteristic of the nanowires cannot be attributed to CB oscillations. They rather remind of features seen in Figs. 19 and 20 at high top-gate voltages ($V_{TG} > 9$ V), where the CB conductance oscillations vanish. These features also resemble those observed by Leobandung et al. in similar quantum dot structures [8] and can be interpreted in terms of electron interference effects within the nanometer-scale structured 2DES.

In order to demonstrate the effect of the in-plane side-gate, we measured the conductance of the 25 nm wide wire as a function of side-gate voltage V_{SG} at a fixed top-gate voltage of $V_{TG} = 12$ V, which is large enough to drive both side-gate and wire into strong inversion. In Fig. 25(b) the decrease of the conductance with V_{SG}

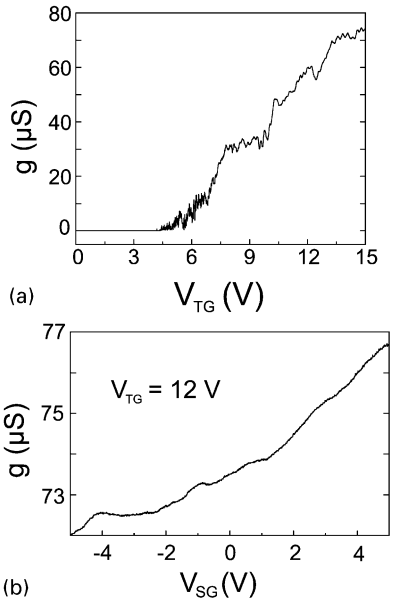

Fig. 25. (a) Gate characteristic of a 25 nm wide and 500 nm long wire. The features observed can be interpreted as electron interference effects, since no Coulomb blockade diamond could be found. (b) Conductance of a strongly inverted 25 nm wide wire as a function of V_{SG} at fixed $V_{TG} = 12$ V.

<0 V and the increase with $V_{SG} > 0$ V demonstrates the feasibility of depleting and enhancing the electron channel inside the nanowire.

In conclusion, single-electron transistors built in the inversion channel of a SOI-MOSFET provide better control of the tunnel barriers compared to highly doped silicon nanostructures, which is mandatory for high-temperature operation of SET devices. With this technique, SET devices operating at room temperature may become feasible.

6.4. An electron waveguide

As shown in Section 2, electron waveguide devices consisting of narrow electron channels with lengths below the elastic and inelastic mean free path of the electrons display distinct steps in the conductance as a function of V_G. These steps can also serve as a nanometer scale switch operating at room temperature, when the lateral dimensions come in the range of about 10 nm. Here, we present one realization of a similar electron waveguide consisting of a very narrow but long SOI-nanowire as shown in Fig. 7 embedded into an inversion SOI-MOSFET. Fig. 26 shows the gate characteristic of this nanowire with a nominal width of 10 nm and a length of 500 nm. The height of the wire is about 20 nm. In contrast to the results on the inversion quantum dots and the wider quantum wire, the threshold voltage for electronic conduction is clearly shifted to higher values of V_{TG}.

In Fig. 27 the nonlinear source–drain characteristic as a function of V_{TG} is shown in a grey-scale contour plot. Though no Coulomb blockade diamond can be seen, a distinct conductance minimum appears at zero bias indicating a conductance blockade not caused by Coulomb repulsion. The Fermi wavelength of the electrons incident into the wire can be estimated from the two-dimensional electron density at a given gate voltage. In the gate voltage range of interest, this yields a λ_F^{2D} which is of the same order as the wire width. We conclude, that even above the normal threshold

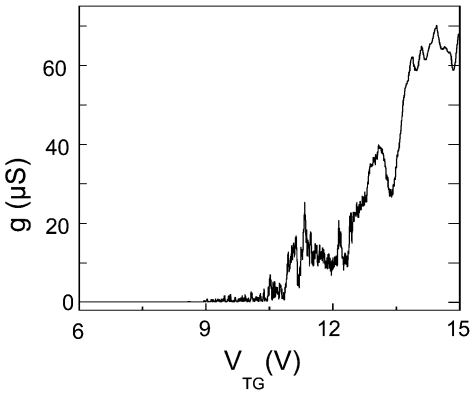

Fig. 26. Gate characteristic of a 10 nm wide, 20 nm high and 500 nm long silicon quantum wire. Electron conductance starts at a threshold voltage much higher than for similar quantum dot structures.

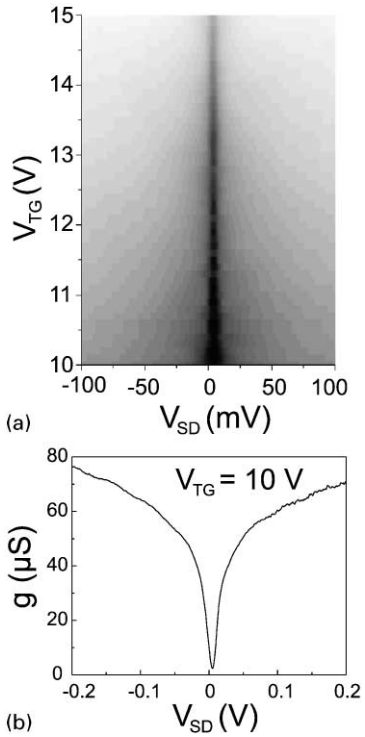

Fig. 27. Nonlinear gate characteristic of the 10 nm quantum wire in a grey-scale contour plot. No Coulomb blockade diamond is visible though a distinct conductance minimum around zero bias can be seen that decreases with increasing V_{TG}.

voltage the two-dimensional electron wave function does not fit into the wire as long as λ_F^{2D} is larger than the wire width. Raising V_{TG} above that value, electron transport through the wire becomes possible. Alternatively, electron transport can be triggered by raising the source–drain voltage V_{SD} to sufficiently high values. In conclusion, the quantum wire presented here acts as an electron switch which does not rely on Coulomb blockade effects but rather on the spatial extension of the electron wave function.

7. Suspended silicon nanostructures

Underetching of lithographically defined SOI-nanostructures leads to a suspension of these devices and therefore to a thermal decoupling from the silicon substrate. Locally, the buried oxide can be easily removed in buffered hydrofluoric acid. To avoid damage during the drying process, we employ a critical point drier. The exact fabrication process of these devices is described in detail elsewhere [48]. In Fig. 28(a),

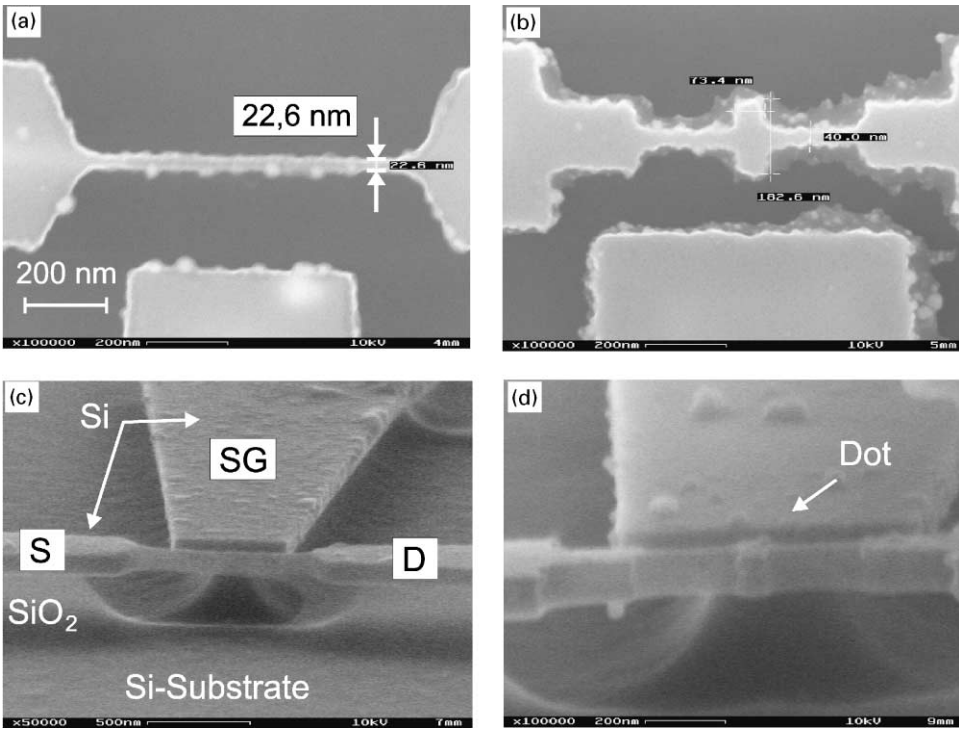

Fig. 28. (a) SEM-micrograph of a suspended silicon nanowire with dimensions of only 23 nm × 80 nm × 800 nm (width × thickness × length). Below the silicon nanostructure, the remaining buried oxide is visible, which functions as the mechanically supporting structure (b). The side-gate was defined in order to control the conductance of the highly doped nanowire. (c) SEM-micrograph of a suspended silicon dot structure with an area of 70 × 180 nm^2. The sideview in (d) proves the complete removal of the underlying oxide.

an SEM-micrograph of our smallest suspended silicon wire so far is shown in a topview. This wire is made out of highly doped SOI and has a width of 23 nm, a thickness of about 80 nm and a length of 800 nm. Fig. 28(b) shows that the wire is completely suspended and only the large source- and drain contacts are supported by the buried oxide. In Fig. 28(c), a similar SEM-micrograph of a suspended, highly doped quantum dot structure with an area of 70 × 180 nm^2 is presented. As for the wire, a sideview in Fig. 28(d) demonstrates the total underetching of this structure.

7.1. Suspended nanowires

Fig. 29 shows the nonlinear transport characteristic of a 40 nm wide and 140 nm thick suspended nanowire similar to that shown in Fig. 28(b) as a function of temperature T. A clear minimum of the conductance around zero bias $V_{SD} = 0$ V

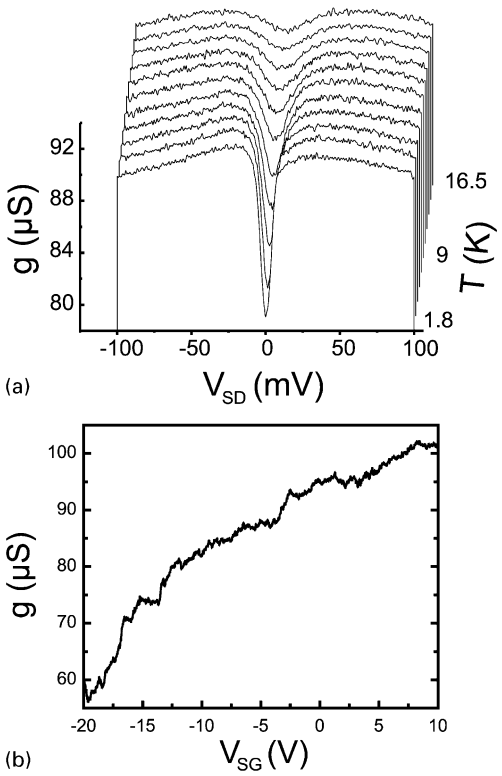

Fig. 29. (a) Temperature dependence of the conductance of a 40 nm wide and 140 nm thick suspended wire. Coulomb blockade is observed at $V_{SD} = 0$ V. The conductance minimum remains visible up to temperatures of about 20 K. (b) Conductance as a function of V_{SG}. The nanostructure cannot be depleted fully.

can be observed up to temperatures of about $T = 20$ K. As can be seen, this conductance dip does not decrease to zero as would normally be expected from conventional Coulomb blockade theory. In contrast to nonsuspended highly doped SOI-nanostructures, where the conductance can be tuned to zero by depleting the wire with a metallic top-gate, in the suspended nanostructures reported here the carrier density can be controlled only by a suspended side-gate machined out of the highly doped SOI-film. In Fig. 29(b) we show the side-gate voltage dependence of the conductance of the suspended nanowire. Obviously, this side-gate depletes the wire and decreases the conductance by about 40%, but cannot tune it close to zero. Presumably, the tunnel junctions formed by a random dopant distribution still provide relatively strong coupling of individual electron islands and, consequently, prevent a complete blockade at $V_{SD} = 0$ V resulting in zero conductance.

In Fig. 30(a) the nonlinear characteristic is measured in a wide voltage range up to $|V_{SD}| = 1$ V. Contrasting measurements of similar nonsuspended structures [43]

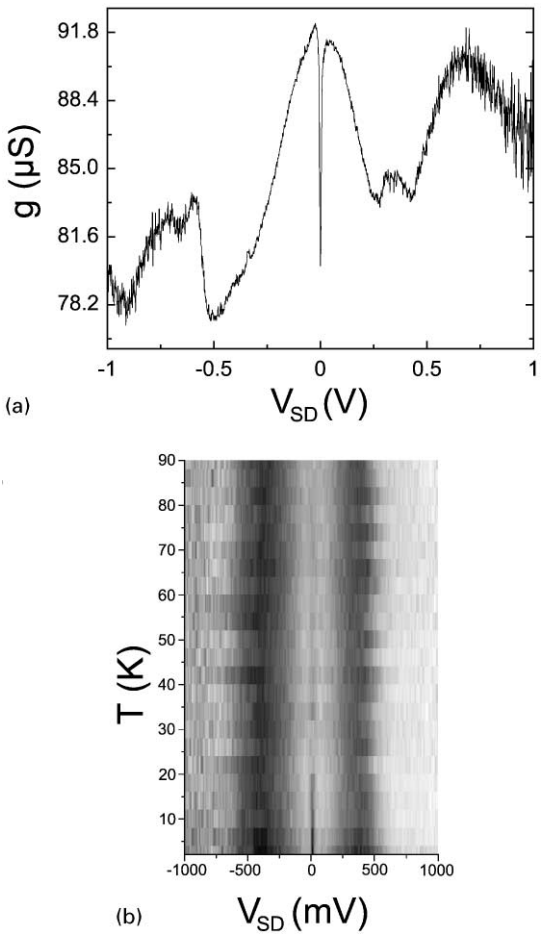

Fig. 30. (a) Conductance of the suspended nanowire at high V_{SD}. (b) A strong modulation can be seen that does not change with temperatures up to 90 K.

(Section 5), a strong modulation of the characteristic at high V_{SD} can be found. This modulation cannot be explained in terms of conventional Coulomb blockade theory. Moreover, this modulation turns out to be almost independent of temperature as is shown in the grey-scale plot of Fig. 30(b). We interpret this observation in terms of phononic influences on the electron transport. The electronic contribution to the thermal conductance of the highly doped SOI-film estimated using the Wiedemann–Franz law is orders of magnitude smaller than the phononic contribution. Heat transport through the suspended wire is therefore mainly carried by phonons. When an electric current is fed into the structure, the suspended nanowire heats due to dissipative ohmic losses until an equilibrium between heat production and heat flow from the wire into the leads is reached. As a function of the wire temperature, different phonon modes can be excited with a phonon energy $\hbar\omega \approx kT$. At a given

temperature $T(V_{SD})$ the number of excitable phonons depends on the density of states $Z(\omega \approx kT/\hbar)$. Therefore, the inelastic electron–phonon scattering becomes a function of V_{SD}. For $V_{SD} \approx 1$V the phonon energy comes close to the boundary of the Brillouin zone, where a strong modulation of the density of states can be found (van Hove singularity) [49]. In our opinion, the measured modulation of the conductance at large V_{SD} therefore may directly reflect the phononic density of state. Since the temperature of the wire is several 100 K at $V_{SD} \approx 1$ V, the absent influence of the VTI-temperature on the conductance up to 90 K can be understood.

7.2. Suspended dot-structure

Fig. 31(a) shows the bias-dependent conductance of the suspended quantum dot device (Fig. 28(d)) at $T = 2$ K. Here also a conductance minimum is found at $V_{SD} =$

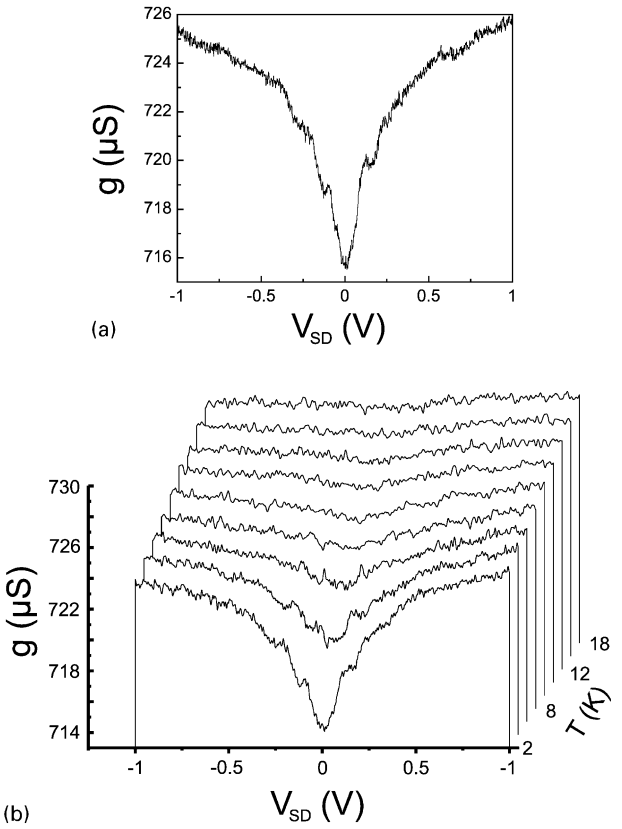

Fig. 31. (a) Conductance of a suspended quantum dot structure as a function of V_{SD}. Nonohmic behaviour is seen around $V_{SD} = 0$ V, indicating single-electron effects. An almost periodic finestructure is superimposed. (b) Temperature dependence of the conductance. The conductance dip at zero bias vanishes with increasing temperature.

0 V which is reminescent of Coulomb blockade found in similar supported structures [10,43]. In addition, an almost periodic fine structure not found in the supported counterparts is superimposed on the conductance dip at zero bias. The temperature dependence of the conductance is shown in Fig. 31(b). The conductance minimum at zero bias vanishes at temperatures of about 8 K. Applying a depleting side-gate voltage $V_{SG} < 0$ to the in-plane gate leads to a reduced conductance of the suspended nanostructure but cannot deplete the device completely. Hence, as for the suspended wire, we are not able to observe a distinct conductance gap at $V_{SD} = 0$ V. As a function of temperature, the observed fine structure did not change in position along the V_{SD}-axis. Also, no change has been observed as a function of V_{SG}. On the other hand, the fine structure observed at low temperatures vanished in relatively low magnetic fields of $B < 1$ T. In suspended nanostructures the phonon-gas experiences a reduction in dimensionality when the phononic wavelength λ_{ph} becomes of the order of the typical structure size [50]. In metallic wires λ_{ph} can be approximated to

$$\lambda_{ph} \approx \frac{v_S h}{2kT}. \tag{7.1}$$

Applying this relation to the quasi-metallic SOI-films used in this work and assuming the velocity of sound v_S in silicon to be between 4500 m/s for acoustic surface modes and 9000 m/s for bulk modes at $T = 4$ K [48], λ_{ph} is found to lie between 55 and 110 nm, respectively. Therefore, a dimensional reduction for phonons may play an important role also in this suspended nanostructure. A cut-off energy E_c for phonons in one-dimensional wires can be computed from the solution of the scalar wave equation for an isotropic medium [50]. For nanowires with cross-sections of 40 nm $\times$ 80 nm one derives $E_c \approx 0.25$ meV corresponding to a temperature $T \approx 2.5$ K. Since therefore at low temperatures ($T < 2$ K) the excitation and propagation of phonons should be suppressed in the suspended nanostructure, the electron–phonon scattering $1/\tau_{eph}$ rate should also be lowered. As a consequence, electron interference effects caused by electrons reflected from the boundaries of the suspended structure may be made responsible for the observed fine structure. Due to the special shape of our device resembling a Fabry–Perot interferometer, electrons reflected from the frontside of the rectangular quantum-dot structure presumably can interfere with incoming electrons propagating in the opposite direction.

In summary, suspending silicon nanowires leads to the observation of novel effects in single-electron transport. Suspended devices are particularly suited for the study of electron–phonon interactions.

8. Summary

In this review we present measurements on single-electron devices fabricated out of highly doped SOI, devices realized in quasi-metallic SOI and devices embedded in inversion field-effect structures. They all show single-electron effects such as Coulomb blockade. The electrical properties of the different single-electron devices are compared. Silicon quantum dots in SOI-MOSFETs are the most promising

candidates for room-temperature operation, whereas highly doped and especially quasi-metallic structures allow a better control of the periodicity of the conductance oscillations. We have further demonstrated a novel kind of silicon nanostructure: the suspended SET (SUSET). By suspending highly doped silicon nanowires or geometrically defined dots, one can observe single-electron effects in thermally decoupled nanostructures. These devices allow a new class of experiments investigating the combination of phonon quantization and single-electron tunneling.

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