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Single-electron tunneling in silicon nanostructures

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Abstract. We present a brief overview on different realizations of single-electron devices fabricated in silicon-on-insulator films. Lateral structuring of highly doped silicon films allows us to observe quasi-metallic Coulomb blockade oscillations in shrunken wires where no quantum dot structure is geometrically defined. Embedding quantum dot structures into the inversion channel of a silicon-on-insulator field-effect transistor Coulomb blockade up to 300 K is observed. In contrast to the quasi-metallic structures, in these devices the influence of the quantum mechanical level spacing inside the dot becomes visible. Suspending highly doped silicon nanostructures leads to a novel kind of Coulomb blockade devices allowing both high-power application as well as the study of electron–phonon interaction.

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Conventional complementary metal-oxide-silicon (CMOS) technology will, as is commonly assumed, reach its physical limits in the near future. Therefore, the search for a new kind of nanoscale devices for integrated circuits is nowadays one of the most challenging tasks. Especially single-electron devices such as single-electron transistors (SETs) are believed to be able to replace standard field-effect transistors (FETs) in the nanoscale regime. However, two conditions must be satisfied to successfully integrate single-electron devices in standard technology: (i) the devices have to work at room temperature, which requires that their geometrical dimensions are on the order of 5 nm as will be explained later and (ii) the choice of silicon for fabricating the structures is mandantory for compatibility and integrability. Especially silicon-on-insulator (SOI) materials, where a thin film of crystalline silicon is located on top of an insulating layer separating the silicon film from the underlying substrate, are the most promising candidates for such silicon-based SET structures. Up to now, several different types of single-electron devices based on SOI or similar structures have been proposed and realized [1–3], leading to first SETs working at room temperature [2, 4].

The purpose of this article is to review some of these attempts, to compare their physical properties and to present our results. In the first section, a brief introduction to the theoretical framework of single-electron tunneling is given. The second section focuses on the preparation of SOI-based single-electron structures using high-resolution electron-beam lithography. The two major kinds of SET devices that can be realized in SOI are presented in the next two sections: a high doping level of the SOI film in combination with lateral structuring of the film leads to the formation of a serial arrangement of randomly distributed SET structures in ultra-small silicon nanowires. Especially by choosing extremely high doping levels (achieved by ion implantation), metal-like Coulomb blockade (CB) oscillations can be observed in these devices. Using geometrically defined SET structures embedded in the inversion channel of a SOI-MOSFET, also allows us to observe CB in these semiconductor quantum dots. In contrast to the quasi-metallic behavior of the highly doped devices, these quantum dots show strong quantum effects resulting from confining few electrons in a box smaller than the electronic Fermi wavelength λ_F. The last section deals with a novel kind of silicon-based SET devices: nanomachining of highly doped silicon nanowires or quantum dot structures is used to suspend single-electron structures. Since these suspended devices are thermally decoupled from the underlying semiconductor substrate, phonon–electron interaction mechanisms can be studied. Moreover, the possibility of simultaneously using these devices for electron transport measurements and to excite them to mechanical vibration, allows the study of electron–phonon interaction, especially when cooling the structures down to temperatures of a few mK. As will be shown, these devices are also very robust against the use of high electrical power, presumably allowing high-power devices on the nanometer scale.

1 Single-electron tunneling

Single-electron tunneling through a quantum dot occurs when the electron island is weakly coupled to source and drain leads. In order to maintain discrete energy states inside the dot, the energetic uncertainty due to lifetime broadening has to be much smaller than a typical interaction energy in the dot. Since electron flow onto the dot is suppressed by Coulomb repulsion this energy scale will be the Coulomb

charging energy E_C:

$$E_C = e^2/C\,. \tag{1}$$

with C being the total capacitance of the electron island. Approximating the lifetime by a RC time-constant leads to the condition for single-electron flow via source and drain contacts:

$$R \gg h/e^2\,, \tag{2}$$

with R being the resistance of the tunnel contacts and h Planck's constant. In other words, electrons have to tunnel successively onto and from the dot in order to resolve single-electron effects. On the other hand, tunneling through the electron island can only occur when the source and drain chemical potential μ is aligned to one quantum dot state, leading to the expression

$$E(N+1) = E(N) + \mu_N\,, \tag{3}$$

where $E(N)$ gives the total energy of the electron system inside the dot occupied with N electrons and μ_N its chemical potential (Fig. 1a). This condition leads to a series of conduction peaks in the gate-voltage/current characteristic of a quantum dot whenever the gate voltage V_G aligns the dot's chemical potential μ_N, μ_{N+1} ... to the source and drain chemical potential μ_F. The electron energy $E(N)$ contains both the electrostatic Coulomb energy as well as the single-particle energies E_N due to the quantum mechanical confinement of the electron wavefunction inside the small electron island. With C_G being the capacitance between the gate and the quantum dot one can derive an expression for the spacing ΔV_G between two conductance peaks in the gate characteristic [5]

$$\Delta V_G = \frac{1}{e}\frac{C}{C_G}\left(\delta E_N + \frac{e^2}{C}\right)\,, \tag{4}$$

with $\delta E_N = E_{N+1} - E_N$. The conversion factor α links the peak spacing as a function of V_G to the energy scale

$$\Delta\mu = \alpha\Delta V_G = e\frac{C_G}{C}\Delta V_G\,. \tag{5}$$

By applying a non zero voltage to source and drain one measures the nonlinear transport characteristic of the quantum dot device. Since a difference of the source and drain chemical potentials allows current to flow through the dot as long as an energy level falls into this gap, the conduction peaks become broader (Fig. 1b). Plotting the conductance of the dot against both gate-voltage and source-drain bias therefore leads to the so-called Coulomb blockade diamond (Fig. 1c). The conversion factor α can be determined by evaluating the slope of the CB diamond

$$\alpha = \frac{1}{2}e\,\mathrm{d}V_{G,\diamond}/\mathrm{d}V_{SD}\,, \tag{6}$$

with $V_{G,\diamond}$ representing the edge of the diamond. From the temperature-dependent shape of the conduction peaks with a FWHM $\Delta V_{1/2}$ one can also extract a value for α and therefore the charging energy [5, 6] of the quantum dot structure

$$\alpha = \frac{5k_B\Delta T}{e\Delta V_{1/2}}\operatorname{arcosh}\sqrt{2}\,. \tag{7}$$

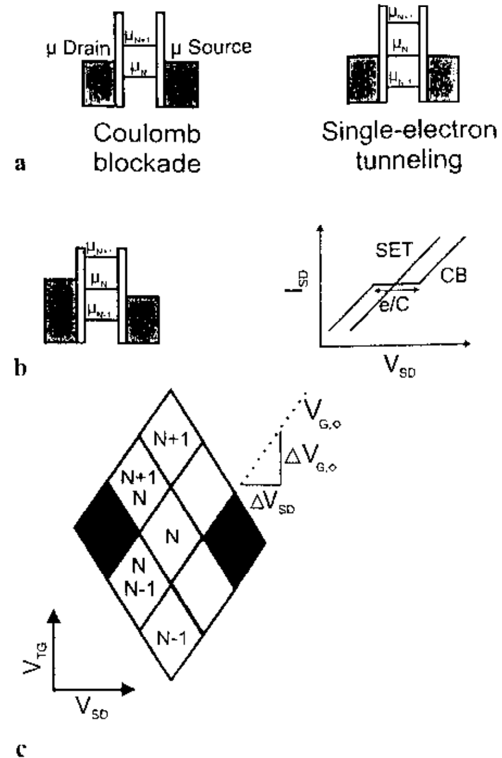

Fig. 1. **a** Coulomb blockade in a single-electron transistor: if the chemical potential of the source and drain leads are not aligned to an energy level inside the electron island (Coulomb blockade), no can current flow through the dot. Only when the chemical potential is aligned to one energy level (single-electron tunneling) or if one energy level lies in the gap between the chemical potentials of source and drain (**b**) can current flow. These two effects lead to the observation of the CB diamond sketched in **c**. In semiconductor quantum dots the electron confinement inside the dot leads to influence of the quantum mechanical energy states for the electrons. Therefore, the energy levels due to the Coulomb interaction are split into a series of levels separated by the quantum-mechanical single-particle energies (not shown here for clarity). In the case of ultrasmall dots in the 10-nm regime, the quantum-mechanical energy spacing becomes of the same order as the Coulomb energy and no clear periodicity of the energy states inside the dot can be expected

The possibility of switching between a conducting state and the CB state of the quantum dot by applying an appropriate gate voltage makes this device a prime candidate for a single-electron switch or memory. In the metallic limit, where the spatial quantization energy is neglibible in comparison to the Coulomb energy, the conductance peaks become equidistant and the CB oscillations perfectly periodic. This is the case for an occupation of the dot with many electrons similar to single-electron transistors in metallic systems [7]. For silicon, this limit can be almost reached by using a very high doping level. When the quantum dot is occupied with only a few electrons, the quantum mechanical energy spacing $\delta\varepsilon_N$ becomes significant in small quantum dots and alters the periodicity of the CB oscillations, as observed with silicon quantum dots embedded in the inversion channel of field effect transistors. In this case, the energy levels due to Coulomb repulsion split into a series of levels separated by the quantum-mechanical

single-particle energy. For silicon dots in the inversion layer of SOI-MOSFETs the quantum-mechanical single-electron energy spacing can be comparable to the Coulomb energy and therefore no periodicity of the energy states inside the dot can be expected.

2 Fabrication of silicon-based nanostructures

Since state-of-the art optical lithography is still limited to structure sizes down to about 180 nm [8], other high-resolution lithography techniques such as electron-beam lithography are needed in order to define features in the 10 nm range. However, even with today's best electron-beam lithography using field-emitting electron sources, fabricating structures with dimensions about 10 nm is difficult to achieve. Since the resolution limit of electron-beam lithography is mostly set by the sensitivity of the electron resist, novel kinds of high-resolution resists have been investigated. Recently, Fujita et al. [9] demonstrated how to use the negative electron resist calixarene to define structures with dimensions of about 10 nm. However, this resist has to be exposed with high electron doses leading to severe irradiation damage especially if using high electron energies. Therefore, low-energy electron-beam lithography has attracted considerable interest in the past few years [10] and is becoming especially interesting for calixarene: using low electron energies leads to drastically reduced electron doses during exposure as can be estimated using a simplified Bethe equation. Furthermore, in combination with the lower electron dose, the low electron energy leads to a strong reduction of irradiation damage [11]. In Fig. 2, a SEM micrograph of a nanowire patterned in a 40-nm-thick calixarene film using a 10 keV electron beam is shown. Although the resolution limit of calixarene due to its chemical structure should clearly be lower than 10 nm, adhesion of the resist to the underlying substrate leads to minimal structure sizes of about 8 nm.

We start the fabrication of our devices by doping the SOI wafers by ion implantation of As. For the highly doped SET devices a uniform doping of the whole wafer is employed.

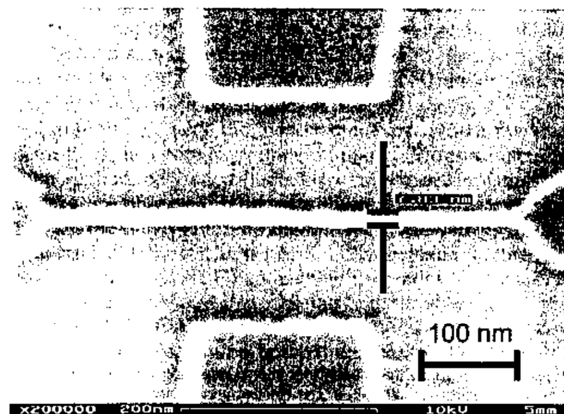

Fig. 2. Nanowire with a width of 8 nm defined in calixarene. Due to adhesion problems of the resist to the substrate, this structure size is believed to be the practical resolution limit for this resist

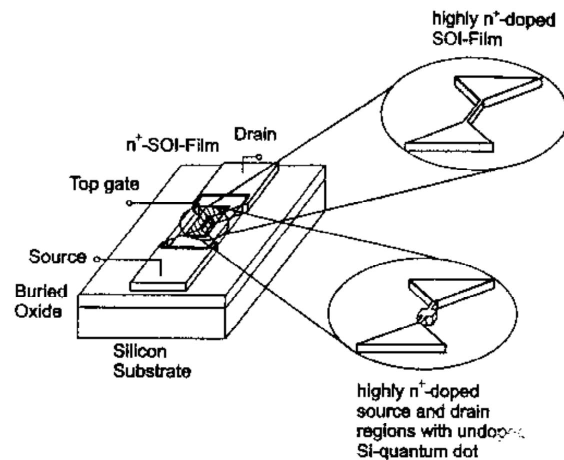

Fig. 3. Sketch of a SOI nanowire embedded in a MOS structure. This MOS device can either be realized in a uniformly doped SOI wafer or in a conventional inversion MOS-architecture, where only the source and drain regions are selectively n^+ doped

In order to fabricate inversion-MOS structures, we mask the areas of the active MOS structures by conventional photoresist. When employing low-energy electron-beam lithography with calixarene to fabricate SET structures in SOI films, the exposed resist film is used as an etch mask for a reactive ion etching process (RIE) which removes the unprotected silicon layer down to the buried SiO_2. Since the calixarene resist has a lower etching rate in the CF_4 plasma than silicon, the masking is suitable for structuring SOI films up to a thickness of about 50 nm. Large contact regions are protected by a photoresist masking during the RIE process. We subsequently grow a thin thermal gate oxide at a temperature of 950 °C in order to passivate the etched structures and to anneal etching damage at the structure surfaces. We then deposit a second oxide film either by chemical vapor deposition or by sputtering and provide a metallic top gate by evaporation or sputtering. This fabrication process can either be applied to uniformly highly n^+-doped SOI wafers or to slightly p-doped layers suitable for inversion-MOS-structures, where only the source and drain regions are highly n-doped by selective implantation. Figure 3 shows a sketch of both a highly doped silicon nanowire as well as a silicon quantum dot in an inversion layer embedded in a MOS structure as described above.

3 Single-electron tunneling in highly doped silicon nanostructures

Smith et al. [3] first fabricated conducting silicon nanowires with lateral dimensions down to about 40 nm using highly doped SOI material. It was possible to resolve conduction peaks when changing the voltage applied to an in-plane side gate also realized in the highly doped SOI film. Although the mean peak-to-peak spacing was constant in subsequent gate sweeps, both the exact peak positions as well as the peak amplitudes differ. This observation can be interpreted in terms of the formation of randomly distributed electron islands separated by tunneling barriers formed by dopant fluctuation

inside the nanostructure. Since usually a serial arrangement of SETs is formed, no exact periodicity of the conduction peaks can be found in these structures. Besides, an enhancement of the Coulomb gap has been observed in the case where the highly doped silicon nanostructure is almost depleted by the side-gate voltage [12]. This behavior is attributed to the formation of space-charge regions (SPR) in series with the tunnel barriers formed by random dopant fluctuations [13]. Recently, also single-electron effects in vertical SETs were observed [14].

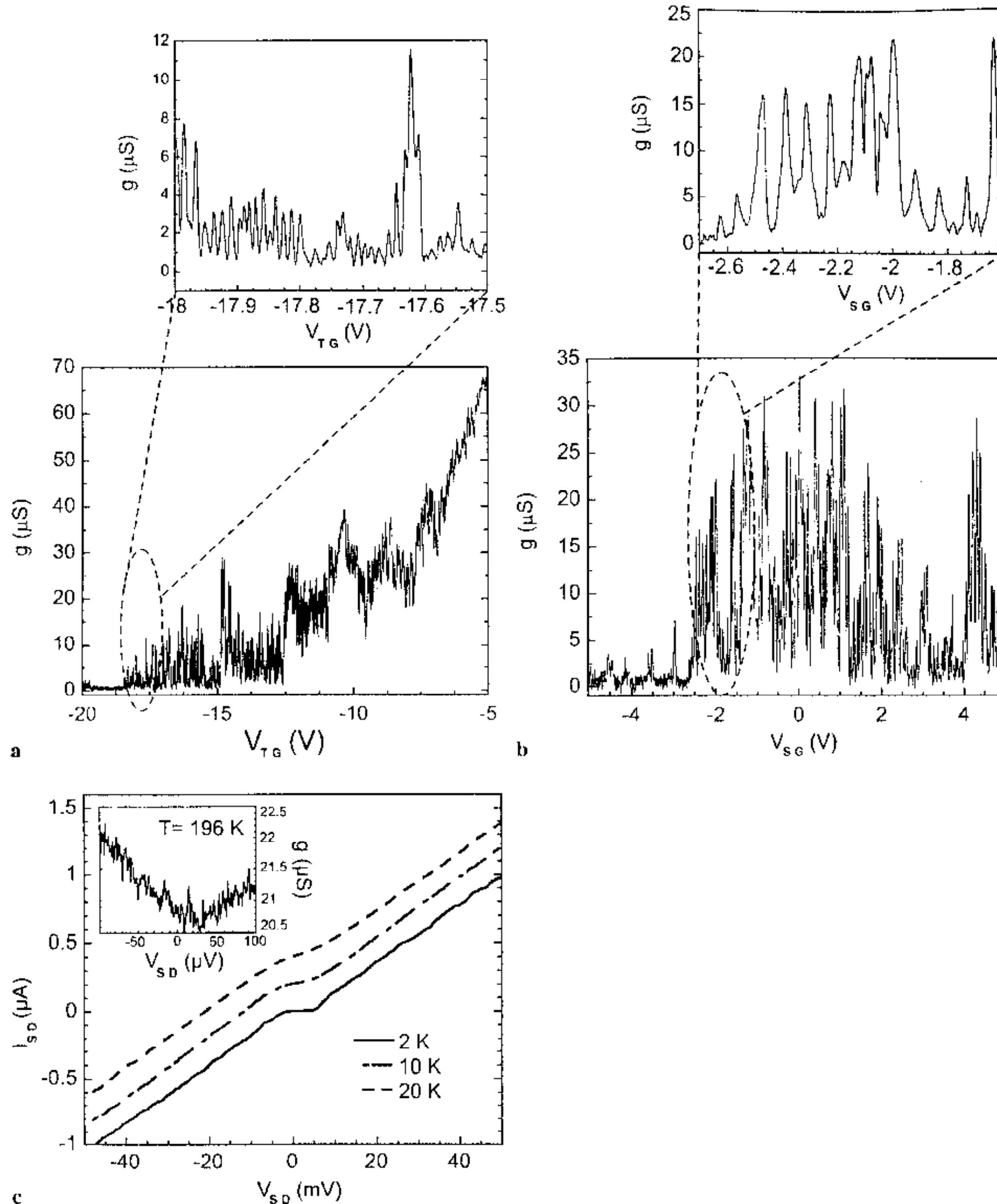

Fig. 4a–c. Single-electron effects in a highly doped, 10-nm-wide silicon nanowire at $T = 2$ K. Although almost periodic conductance oscillations can be found, both the peak amplitudes as well as the exact peak positions differ between subsequent gate sweeps. **a** The electrostatic potential of the nanowire is controlled via a metallic top gate. **b** An in-plane side gate is used. The top-gate voltage in this measurement is $V_{TG} = 17.5$ V, allowing low side-gate voltages to control the CB oscillations. **c** The temperature dependence of the wire's $I - V$ trace. Although single-electron effects should remain visible up to temperatures above 200 K due to the small size of the structure, the wire almost shows ohmic behavior already at lower temperatures and single-electron effects remain visible only weakly up to temperatures of about 200 K

In Fig. 4, we present CB oscillations measured in a silicon wire of width 10 nm and thickness around 25 nm (after shrinking by thermal oxidation) which is similar to that previously mentioned [3]. In contrast to the common side-gate configuration, in our setup both one side-gate as well as a metallic top-gate can tune the electrical potential inside the highly doped wire. In Fig. 4a the conductance of the wire, $g = \mathrm{d}I_{SD}/\mathrm{d}U_{SD}$, is plotted versus the depleting top-gate voltage V_{TG} at a temperature of $T = 2$ K. By setting the top-gate voltage to a value near pinch-off, one can observe CB oscillations by changing the side-gate voltage V_{SG} (Fig. 4b). This allows us to minimize the controlling side-gate voltage. The temperature-dependent conductance of the silicon wire as well as of the SET structures treated in the following sections were measured in a ^{4}He bath cryostat with a variable temperature insert, allowing continuous operation in the range 1.5–200 K. In Fig. 4c, the temperature dependence of the source-drain $I - V$ characteristic is shown. Although single-electron effects should remain visible up to very high temperatures due to the small size of the nanowire, only a weak nonlinearity can be observed at temperatures up to 200 K. We therefore conclude that the tunnel barriers formed by random dopant distribution must be very shallow, so that the condition in (2) cannot be fulfilled at higher temperatures. In addition, although many efforts were recently made to use highly doped SOI films for single electronics with structure sizes in the same range as reported here, no roomtemperature operation of these devices have been observed yet [3, 12, 15, 16].

In recent work, we reported on a novel approach applying SOI technology for the fabrication of quasi-metallic SETs in extremely doped SOI films [17]. Since metallic SETs offer many similar charging states and hence a broad range of operating points, this approach is intended to overcome the poor periodicity of the lower doped structures. Whereas doping levels of about $10^{19}\,\mathrm{cm}^{-3}$ were common in earlier work, leading to a mean distance between two dopant atoms of 4.6 nm, our samples have a nominal doping level of $10^{21}\,\mathrm{cm}^{-3}$ realized by ion implantation of arsenic. This leads to a mean distance of only 1 nm between the dopants. Therefore, the distribution of dopant atoms can be assumed to be much more uniform for an unprocessed wafer. The active doping level was determined by Hall measurements to be about $5 \times 10^{20}\,\mathrm{cm}^{-3}$, suggesting that not all dopants were activated during the annealing process performed in a rapid thermal annealing (RTA) chamber at a temperature of 1100 °C [18]. The electron number in an ideal dot with dimensions of about 50 nm fabricated from this material is on the order of 10^5.

Figure 5a depicts the conductance of a 50 nm-wide, 30 nm-thick nanowire at a temperature of 4.2 K as a function of the applied top-gate voltage. Oscillations with a clear periodicity are observed, indicating the metallic nature of the SET. On the other hand, the high offset in the valleys of the conductivity indicates high parallel conductance. Figure 5b shows a contour plot of the channel differential conductance versus top-gate voltage V_{TG} and source-drain bias V_{SD}. From the slope of the Coulomb blockade diamonds we determine the energy level separation in the dot using (6). For the conversion factor α we obtain the value $\alpha = 0.033\,\mathrm{eV/V}$ and therefore a charging energy of the SET of $E_C = 17.5$ meV. This leads to a total capacitance of $C = 10$ aF. With the straightforward estimation of a cylindrically shaped island with the axis perpendicular to the sample's surface we calculate the island diameter to be about 70 nm. Presumably, the real island formed is larger along the wire than perpendicularly to it. Therefore, this value is in good agreement with the lithographic dimension of the wire.

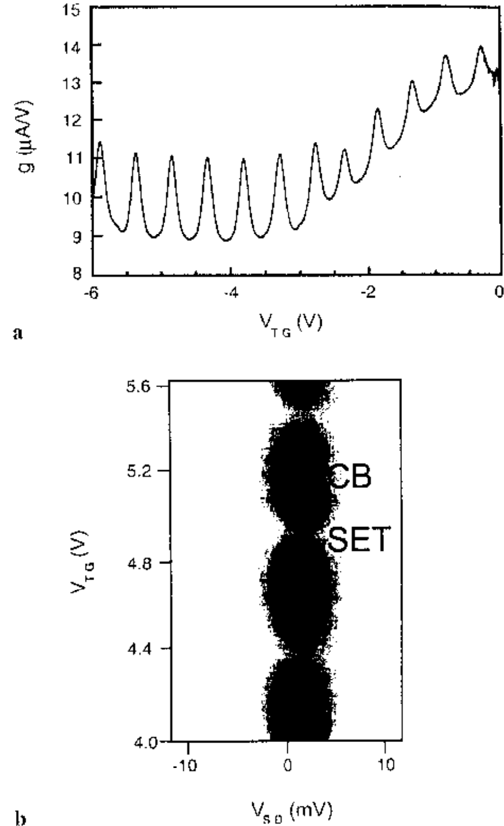

Fig. 5. **a** CB oscillations in a quasi-metallic nanowire showing almost perfect periodicity. **b** CB diamond for the structure measured in (a). From the slope of the diamond the charging energy of the dot formed inside the wire can be estimated

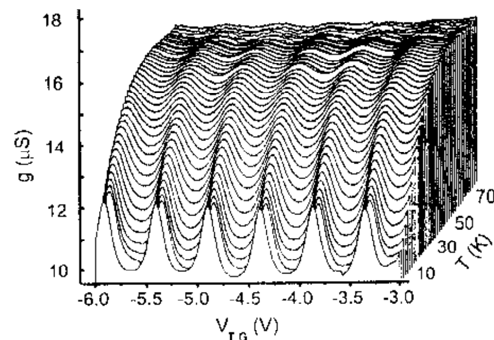

Fig. 6. Temperature dependence of the CB oscillations shown in Fig. 5a. The oscillations remain visible up to temperatures of almost 100 K

In Fig. 6, the temperature dependence of the conductance is presented. The oscillations remain visible up to a temperature above 70 K. Since CB should not be affected unless the thermal energy k_BT exceeds half of the charging energy $E_C = e^2/C$, this result suggests a charging energy of about 15 meV. Furthermore, fitting the shape of the conductance peaks in Fig. 5, one obtains a full-width-half-maximum $\Delta V_{1/2}$ and finds a conversion factor according to (7) of $\alpha = 0.12\,\mathrm{eV/V}$ and a charging energy $E_C = 63$ meV. These values differ strongly from the value calculated using the CB diamond. We believe that the shape of the peaks is influenced by the apparent conductivity of the parallel channel in the nanowire, leading to this deviation [17].

As the doping level of the material is extremely high, it is not reasonable to assume that random dopant fluctuations are able to form single-electron islands inside the nanowires. Presumably, the pattern-dependent two-dimensional oxidation of laterally structured SOI devices in combination with the pile-up effect of As-dopants during dry oxidation and edge roughness of the etched wire leads to the observed SET structure. In fact, since the thermal oxidation of nanometer-scale curved structures is extremely sensitive to the geometry, in particular to the radius of curvature, the oxidation rate can vary significantly along a Si nanowire with some edge roughness [19]. Besides, the As piling up in silicon during dry oxidation due to a segregation coefficient of about 10 [20], presumably also contributes to a very irregular dopant concentration along the wire. Moreover, the formation of SiAs precipitates has been observed under similar conditions [21]. Our observation of a relatively high parallel conductivity can also be explained in this picture, suggesting the formation of a SET at one edge of the wire, whereas at the other edge a wire with ohmic conductance remains.

Although we achieve the formation of single metallic islands in the nanowire presented, we also observed the formation of serial arrangements of metallic electron islands. In this case, the devices show non-periodic conductance oscillations and also an obvious response to a magnetic field applied perpendicular to the wire, as presented in Fig. 7. We believe that the tunneling barriers formed randomly inside the nanowires by segregation effects are affected by a magnetic field in contrast to the very hard potential forming at the Si/SiO_2 interface.

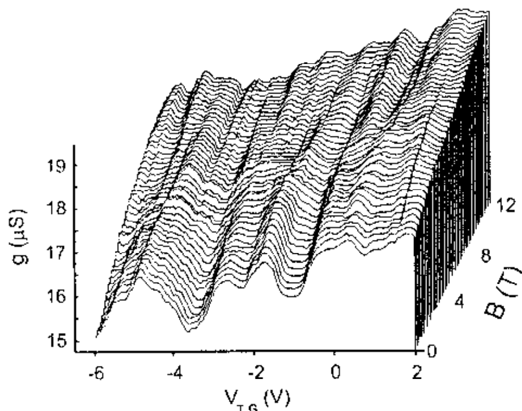

Fig. 7. CB oscillations in a quasi-metallic nanowire. No periodicity is revealed, indicating the formation of a serial arrangement of metallic islands. Although the oscillations of the single islands are almost not affected by a magnetic field indicating a very hard potential wall, the tunnel junctions between adjacent electron islands in the serial arrangement show a strong influence of the magnetic field

In conclusion, the use of both highly doped nanowires as well as of quasi-metallic silicon nanowires allows observation of single-electron effects up to temperatures of about 100 K. Quasi-metallic structures allow the observation of almost perfect Coulomb blockade. Nevertheless, both devices suffer either from poor reproducibility of their electrical properties or from high parallel conductance inside the wires since it is not possible to deplete these extremely doped structures near pinch-off. To further improve the functioning of the quasi-metallic SET devices, one should use geometrically defined quantum dot structures. Since this demands to reduce the conductance through the geometrically defined tunneling barriers, further work is needed and is ongoing at the moment.

4 Single-electron tunneling in inversion-channel quantum dots

In contrast to the use of highly doped SOI films, embedding geometrically defined SET structures into the inversion channel of SOI field-effect transistors allows us to observe CB oscillations up to very high temperatures [1]. Since the tunneling barriers are defined by the geometry, the tunability of these devices is greatly enhanced in comparison with the rather random effects found in highly doped nanowires. The conductance of the barriers can easily be adjusted to fulfill the requirement of (2), by applying an appropriate top-gate voltage. Therefore both problems of high parallel conductances found in quasi-metallic wires as well as shallow barrier potential by a random dopant distribution can be solved. On the other hand, the strong influence of the quantum-mechanical level separation in these semiconductor quantum dots makes an application for single electronics more difficult as in the case of quasi-metallic devices. According to (4) the periodicity of the classical CB is lifted by the influence of discrete energy levels inside a semiconductor quantum dot in the 10-nm range.

Although first successful measurements on these kinds of devices were made on geometrically defined structures [1], also randomly formed single-electron structures were observed recently in SOI nanowires [4] and SOI quantum point contacts [2]. Also in quantum point contacts defined by a stacked-gate geometry in bulk MOS devices using split gates, single-electron effects up to temperatures of about 10 K can be found [22]. The formation of a serial arrangement of electron islands inside a nanowire can easily be understood in terms of edge roughness during the fabrication process. Nevertheless, also in ultrasmall SOI nanowires with widths below 10 nm we did not observe clear CB effects, presumably due to a reduced edge roughness caused by a better electron-beam lithography than reported in the older work [4]. On the other hand, although many efforts were made recently to investigate the origin of SET formation in SOI quantum point contacts [23], the underlying mechanism remains unclear up to now.

We prepared geometrically defined quantum dot structures embedded in SOI-MOSFETs with lateral dimensions of

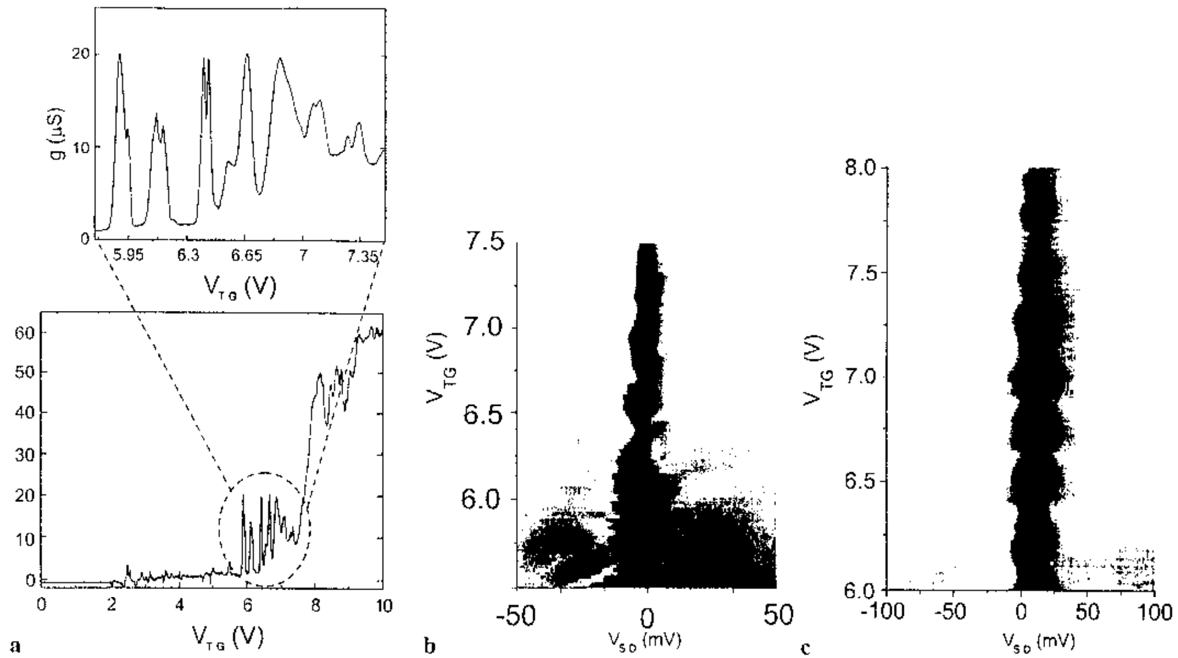

Fig. 8. a Gate-voltage-dependent conductance of an inversion quantum dot at $T = 2$ K. Coulomb blockade is observed near threshold voltage. At higher gate voltages, serial resistances of the source and drain regions become dominant and lead to a saturation of the conductance. b Coulomb blockade diamond of the same structure. Deviations from the classical picture expected for metallic CB are observed, indicating a complicated energy level scheme inside the semiconductor quantum dot. c CB diamond of a similar quantum dot structure. Since this dot is larger and the CB oscillations occur at a higher gate voltage, where the electron number inside the dot is larger, the peak spacings becomes more regular

about 20 nm using the fabrication process described briefly in Sect. 2 [24]. In Fig. 8a, the CB oscillations in a dot with estimated lithographical diameter of 20 nm are presented. As can be also seen in the CB diamond in Fig. 8b, a strong influence of discrete energy levels inside the dot leads to a deviation from the classical periodicity of the oscillations and to a distortion of the diamond shape. From the slope of the diamond and the mean spacing between two adjacent conductance oscillations one can deduce the conversion factor $\alpha = 0.101$ eV/V, the charging energy $E_C = 56$ meV and, assuming a disc shape for the dot, a geometrical dot diameter of $d = 22$ nm. In Fig. 8c the Coulomb-blockade diamond of a somewhat larger dot is shown. For this dot the conductance oscillations are visible at higher gate voltages than for the smaller dot. The above-mentioned calculations now give $\alpha = 0.154$ eV/V, $E_C = 41$ meV and $d = 30$ nm. Therefore, we can assume that the number of electrons inside the dot is larger in this case, which leads to a more classical behavior of this semiconductor dot. Consequently, the peak spacings become more uniform.

Since the charging energy of the smaller dot is found to be very large and $E_C/2$ equals approximately a temperature of 300 K, we expect CB to be visible up to room temperature. In Fig. 9, the $I - V$ characteristic is shown for several temperatures. The inset presents the $I - V$ characteristic as well as the source-drain conductance at 300 K. Since the charging energy decreases for increasing gate voltage (as can be seen in a decrease of the peak separation in Fig. 8a), we measured the $I - V$ characteristic at the relatively low gate voltage of $V_G = 4.5$ V. In the regime where multiple conductance peaks can be found, the lower charging energy does not allow us to expect room-temperature operation. In Fig. 10, we show the temperature dependence of the same quantum dot conductance plotted versus the gate voltage. As can be seen, the first conductance oscillation remain clearly visible at temperatures above 100 K, whereas the oscillations at higher V_{TG} begin

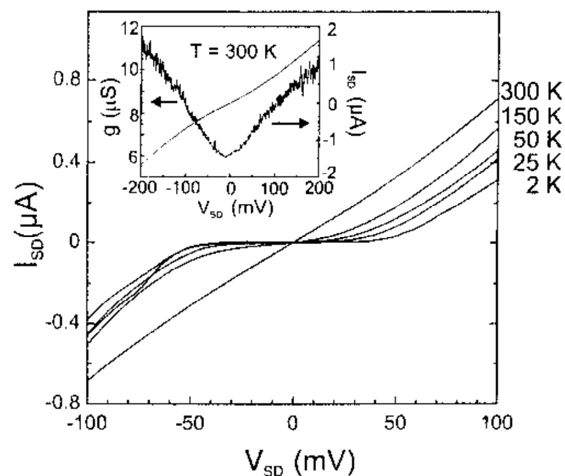

Fig. 9. Temperature dependence of the $I - V$ characteristic of the smaller quantum dot at a top-gate voltage of $V_G = 4.5$ V. *Inset*: clear single-electron effects remain visible at $T = 300$ K

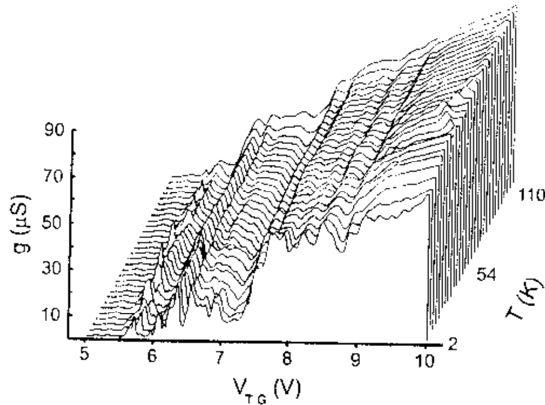

Fig. 10. Temperature dependence of the gate characteristic of the smaller quantum dot. Since the effective size of the dot becomes larger with increasing gate voltage, the oscillations at higher V_G disappear at temperatures higher than 100 K

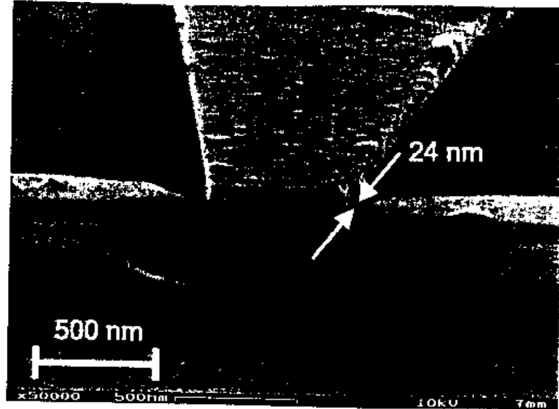

Fig. 11. SEM micrograph of a suspended silicon nanowire measuring only 24 nm × 80 nm × 800 nm (width × thickness × length). Below the silicon nanostructure, the remaining buried oxide is visible, which functions as the mechanically supporting structure. The side gate was defined in order to control the conductance of the highly doped nanowire

to vanish. In our opinion the higher charging energy at low V_G in comparison to that at higher V_G can be explained by a pyramidal shape of the quantum dot structure due to the dry-etch process and the geometry-dependent oxidation. Inverting only the top of the silicon islands leads to a smaller 'electronic' dot diameter and therefore to a lower capacitance to the top gate.

In conclusion, single-electron transistors built into the inversion channel of a SOI-MOSFET enable a better control of the tunnel barriers compared to doped silicon nanostructures, which is mandatory for high-temperature operation of SET devices. In this way, SET devices operating at room temperature become feasible. However, for these, the electronic properties such as the conductance peaks' periodicity are still harder to control than for the metallic counterparts.

5 Suspending silicon nanostructures: a novel approach for nanomechanics and nanoelectronics

Underetching of lithographically defined SOI nanostructures leads to a suspension of the single-electron devices and therefore to a thermal decoupling from the silicon substrate. The buried oxide is removed locally in buffered hydrofluoric acid and, to avoid damage during the drying process, we employ a critical-point drier. The exact fabrication process is described in detail elsewhere [25].

In Fig. 11 a SEM micrograph of our so far smallest suspended silicon wire is shown. This wire is made out of highly doped SOI, has a width of 24 nm, a thickness of about 80 nm and a length of 800 nm. Similarly to the effects described in Sect. 3, single-electron effects are visible in these wires at low temperatures due to random dopant fluctuations . In Fig. 12a, we present the conductance of a 30 nm × 140 nm (cross-section) suspended wire measured at $T = 2$ K. Since it is not possible up to now to reduce the dimensions of these structures below 20 nm, high parallel conductance is present leading to a relatively large offset in the conductance measurement. In addition to the common minimum in the conductance at zero bias, a strong modulation of the conductance at higher source-drain voltages is visible. Although the minimum at zero bias disappears with increasing temperature and is almost not visible at temperatures above 20 K, the coarse modulation remains visible up to temperatures above 100 K as shown in the contour plot of Fig. 12b. This modulation is also insensitive to magnetic fields up to 12 T (not shown here). At the moment, we do not completely understand the electrical behavior of these suspended wires. Work in progress shows other features in the $I-V$ curves of suspended wires and also in geometrically defined suspended dots that have not been found in experiments on similar non-suspended structures. Details of these results will be published elsewhere [26].

Applying a side-gate voltage to the suspended nanowires leads to a reduction in the conductance but does not totally deplete the highly doped structure. A future improvement might be achieved by depositing a metallic layer on top of the side gate in order to obtain a better gating effect and presumably deplete the whole wire. We believe that, similarly to the measurements presented in Sect. 3, the observation of CB oscillations in these suspended nanowires should then become feasible. These devices could then allow us to investigate CB effects in thermally decoupled structures. Moreover, using a setup according to [27], it should be possible to excite vibrational modes in these suspended wires. In this setup, a high-frequency current is fed into the device located in a perpendicular magnetic field where the Lorentz force leads to an oscillation of the suspended wire. In the case of a quantized periodic movement of the wire with respect to the side gate additional conductance peaks in the gate-dependent conductivity should be observable [28]. Moreover, by cooling these structures down to temperatures in the mK regime, phononic effects on the single-electron tunneling will be investigated.

A possible use of suspended nanostructures lies in the field of high-power applications, eventually as suspended FETs. In fact, in our experiments at a temperature of 2 K, the devices were destroyed only after feeding an electrical current through them associated with a power dissipation in-

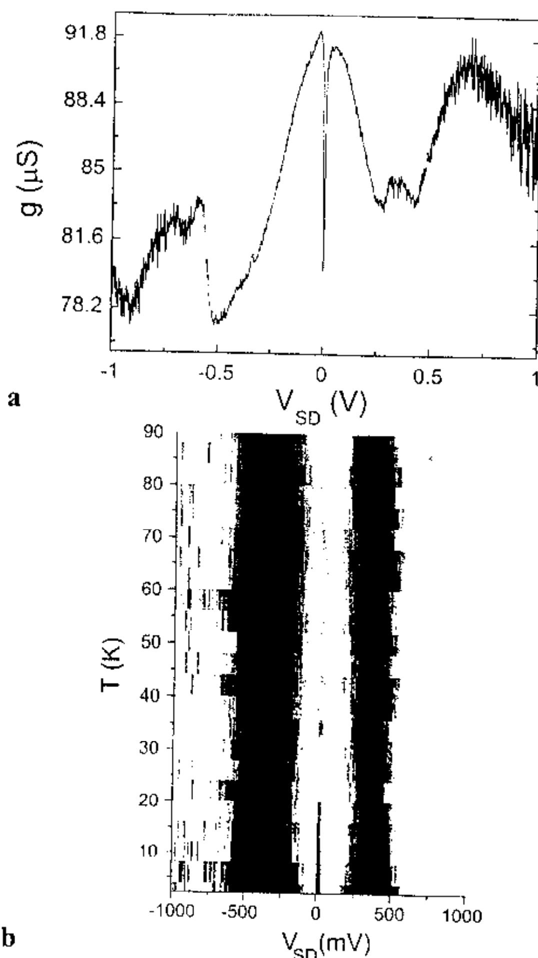

Fig. 12. **a** Conductance of a suspended nanowire similar to that shown in Fig. 11, but measuring 30 nm × 140 nm. The minimum at zero source-drain bias indicates the formation of multiple-tunnel junctions (MTJ) inside the doped wire. **b** The additional structure at higher bias remains unaffected even at temperatures above 100 K

side the suspended part of the nanostructure of 0.3 TW/cm^{-3}. The mechanisms of electrical robustness of these suspended nanostructures constitute a topic of further research.

6 Summary

In this review we present measurements on single-electron devices fabricated in highly doped SOI and in quasi-metallic SOI and the operation of inversion field-effect structures. All the presented devices show single-electron effects such as Coulomb blockade. Their electrical properties are compared. Silicon quantum dots in SOI-MOSFETs are the most promising candidates for room-temperature operation, whereas quasi-metallic structures allow a better control of the conductance oscillations' periodicity. We have further proposed and demonstrated a novel kind of silicon nanostructure: the suspended SET transistor. Suspending a highly doped silicon nanowire or a geometrically defined dot, one can observe single-electron effects in thermally decoupled nanostructures. These devices allow a new class of experiments investigating the combination of phonon quantization and single-electron tunneling.

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