Fabrication and integration possibilities of ultrasmall quantum dots in silicon-on-insulator material

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(Received 15 December 2000; accepted for publication 19 April 2001)

Single-electron transistors utilizing Coulomb blockade effects are promising candidates for future silicon based nanoelectronics. We present the fabrication of such transistors and measurements that reveal Coulomb blockade behavior. Various silicon quantum dots are investigated up to room temperature. We employ a dual gate configuration with which we are able to control our devices by both a metallic top gate as well as by an in-plane gate. This design principle enhances the integration density. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1379352]

I. INTRODUCTION

The ultimate limit of integration is found in single-electron transistors (SETs), which might challenge conventional complementary metal-oxide-silicon (CMOS) technology in the near future. SETs in silicon nano-structures utilize the well established silicon technology thus allowing a large scale integration of these novel devices. In contrast to quantum dots in high-mobility GaAs/AlGaAs heterostructures, where the depletion length of the two-dimensional electron system (2DES) limits the lateral dot sizes to about 50 nm, the use of silicon-on-insulator (SOI) materials comprising ultrathin silicon films allows structure sizes down to 5 nm. Since the capacitance between the quantum dot and the controlling gate structure determines the temperature range in which the SET reliably operates, this miniaturization of quantum dot devices is the most demanding goal for future device applications at room temperature. To date, primarily the two following approaches have been used to realize ultrasmall SOI-SETs: Highly doped SOI films in combination with lateral nanostructuring enable fabrication of conducting silicon nanowires, in which random dopant fluctuations lead to a serial arrangement of multiple tunnel junctions.[1–3] A higher doping level of the order of $N_D \approx 10^{21}$ cm^{-3} leads to the observation of quasimetallic Coulomb blockade (CB) oscillations due to a spontaneous formation of donor precipitates.[4] Leobandung *et al.*[5] and others[6,7] investigated quantum dot structures embedded into the 2DES of an SOI metal-oxide-silicon inversion-field effect transistor [inversion SOI metal-oxide-semiconductor field effect transistor (MOSFET)] and found CB oscillations up to room temperature. The main advantage of these devices compared to the highly doped nanowires lies in the enhanced tunability of the tunnel junctions controlling electron transport onto and off the electron island. So far, only in these inversion SET devices has room temperature operation been reported. Here we present our investigations on quantum dots and quantum wires in inversion SOI-MOSFETs in the sub 10 nm regime. In order to examine the confining potential of the Si/SiO_2 interface of the nanostructure we investigate the electronic properties in high magnetic fields up to 12 T. Since a future integration of these SET devices demands individual electrostatic control of each structure on the nanometer scale we realize a dual gate configuration similar to that reported in Ref. 8. In this arrangement the 2DES in the SOI film is induced by a metallic top gate, whereas the individual single-electron devices can be tuned almost independently by an in-plane gate machined out of the SOI film and driven in strong inversion by the top gate.

II. FABRICATION AND MEASUREMENT SETUP

The unprocessed *p*-type (100)-oriented SOI wafers (specific resistivity $\rho \sim 20\ \Omega$ cm have a silicon film thickness of 50 nm and a buried oxide layer thickness of 400 nm. Protecting the active transistor areas with a standard photoresist, we implant the source and drain regions of the SOI-MOSFET with As ions at an energy of 10 keV and a dose of 2×10^{15} cm^{-2}. In order to obtain thinner silicon films, a sacrificial thermal oxide is grown on the upper Si layer with a thickness of about 44 nm by rapid thermal oxidation (RTO), consuming 20 nm of silicon. After etching the oxide in buffered HF we define a mesa structure in the remaining 30-nm-thick silicon film with alignment marks for the following electron-beam lithography step using conventional photolithography and reactive ion etching (RIE) in CF_4. Using high-resolution low-energy electron-beam lithography and the negative electron resist calixarene,[9] we prepare silicon wires and dot structures with a minimum lateral feature size of about 10 nm by RIE. Simultaneously, the in-plane side gate is formed in the thinned SOI film. The etched silicon structure is passivated by low temperature (950 °C, 16 min) RTO resulting in a high quality oxide of about 15 nm thickness followed by an additional sputter deposition of a 40-nm-thick SiO_2 layer on top of the sample. In a further step we open contact holes in the source and drain regions by wet etching in buffered HF. Finally, metal evaporation and subsequent lift-off serves to fabricate simultaneously bonding pads and a top gate covering both the single-electron structures as well as the side gates. In Fig. 1(a) a schematic drawing of the quantum dot device is shown in combination

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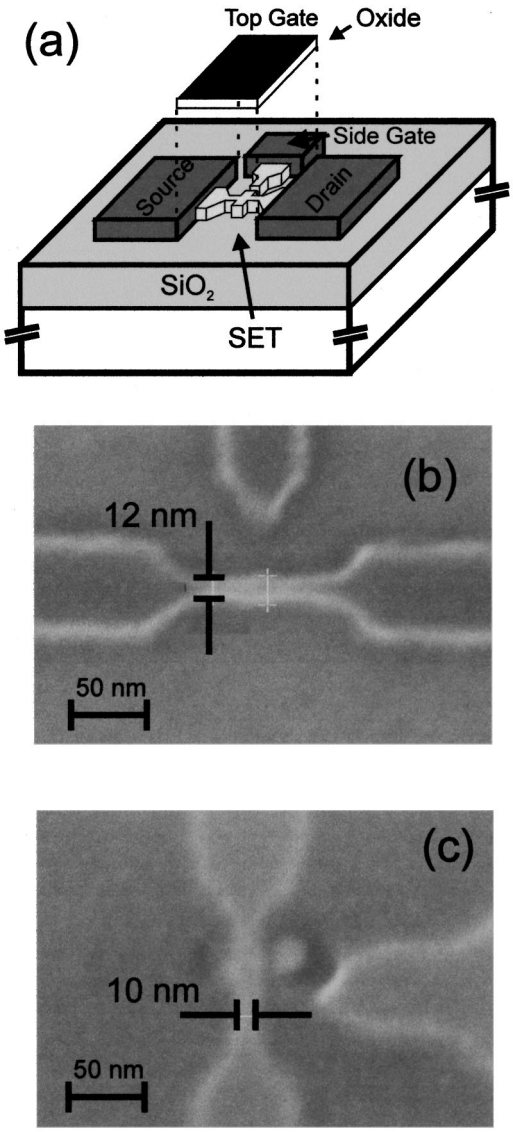

FIG. 1. (a) Sketch of a dual gate quantum dot structure. Highly doped source and drain contacts are connected by the laterally structured inversion layer in the SOI film. An in-plane side gate is also defined in the inversion layer and contacted by a strongly doped region. (b) Scanning electron microscope micrograph of a quantum dot structure. (c) After reactive ion etching of the resist mask, growth of a 15 nm thermal oxide and stripping of this SiO_2 passivation.

with a scanning electron microscope picture of a quantum dot structure (b) defined in calixarene electron resist on a bulk silicon wafer. Figure 1(c) displays the same quantum dot structure etched in silicon, oxidized with the oxide stripped off again in HF in order to demonstrate our preparation technique. After bonding the sample onto a chip carrier and mounting it on a sample holder, the temperature dependence of the electronic properties is measured in a variable temperature insert providing temperatures in the range between 1.5 and 300 K.

III. MEASUREMENTS

A. Quantum dots

In Fig. 2 we show measurements of the conductance, defined as $g=dI_D/dV_{SD}$, for two different quantum dots.

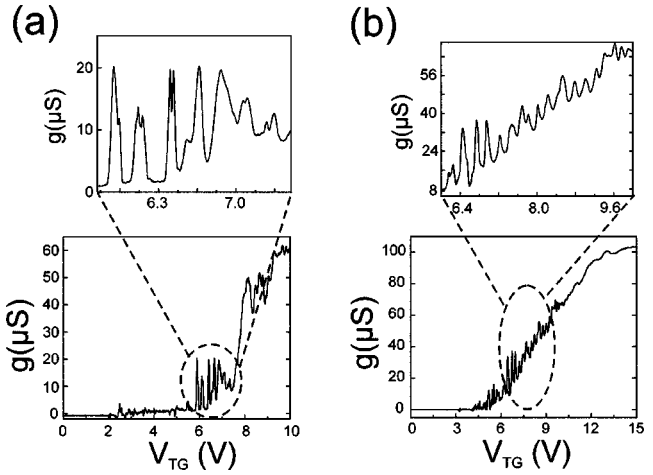

FIG. 2. Coulomb blockade oscillations in two inversion quantum dots at a temperature of 2 K. While the oscillations in (a) (dot 1) display no periodicity with V_{TG}, the peaks in trace (b) (dot 2) are almost perfectly equidistant.

The conductance oscillations found in Fig. 2(a) (dot 1) display no periodicity in contrast to the almost periodic oscillations shown in Fig. 2(b) (dot 2). With C_{TG}, the capacitance of the quantum dot with respect to the top gate, one can derive an expression for the spacing between two conductance peaks in the gate characteristic[10]

$$\Delta V_{TG}=\frac{1}{e}\frac{C}{C_{TG}}(\delta E_N+U) \tag{1}$$

with $\delta E_N=E_{N+1}-E_N$ the separation of the quantized levels caused by spatial confinement. $E_C=e^2/C$ defines the charging energy, namely the energy required to add one additional electron to a quantum dot overcoming the Coulomb repulsion of the electrons already occupying the dot (C being the total capacitance of the dot). In the classical limit, when the spatial quantization energy is negligible in comparison to the Coulomb energy, the conductance peaks become equidistant. This is the case for the occupation of a dot with many electrons, and is similar to single-electron transistors in metallic systems. If a small quantum dot is occupied with only a few electrons, the quantum mechanical energies E_N become significant and alter the periodicity of the CB oscillations. Estimating the quantum mechanical level spacing in the simple approximation of an infinite spherical potential well in Si leads to $\delta E_0 \sim 10$ meV for a dot with a diameter of 20 nm. On the other hand, the Coulomb charging energy can be estimated by the approximation of a disk shaped island with radius r and the axis perpendicular to the surface

$$C_{TG}=8\epsilon_r\epsilon_0 r \tag{2}$$

with ϵ_r the dielectric permittivity for SiO_2 and ϵ_0 the dielectric constant. For a 20 nm dot we obtain $E_C=58$ meV. In Fig. 3 contour plots of the channel conductance versus top gate voltage V_{TG} and source/drain bias V_{SD} of both quantum dots [dot 1 (a) and dot 2 (b)] are shown. From the slope of the so-called CB diamonds one can determine the energy level separation in the dot with the conversion factor $\alpha=\delta\mu(N)/\delta V_{TG}=\frac{1}{2}\Delta V_{TG,\diamond}/\delta V_{SD}$, where $\delta\mu(N)$ is the dif-

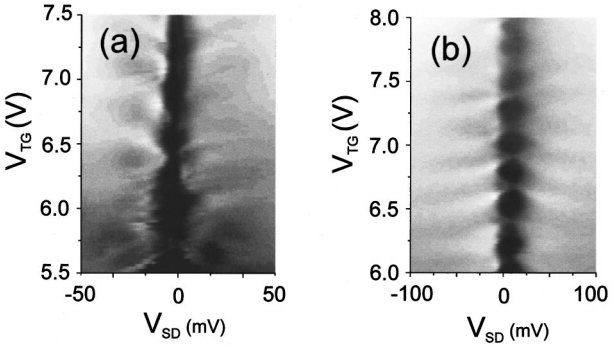

FIG. 3. Contour plots of the channel conductances vs top gate voltage V_{TG} and source/drain bias V_{SD} of both quantum dots are shown. From the slope of the Coulomb blockade diamonds one can determine the energy level separations. The contour plot in (a) (dot 1) displays a variety of fine structures, whereas the Coulomb blockade diamond in (b) (dot 2) almost shows a metallic behavior (black regions indicate the suppression of conductance).

ference of the electrochemical potentials of the dots depending on the number of electrons N.[4] For dot 1 one finds $\alpha \approx 0.101$ eV/V and one can therefore deduce a charging energy of $E_C \approx 56$ meV. With approximation 2 we obtain a dot diameter of $d \approx 22$ nm. On the other hand, regarding the values for δE_0 and E_C estimated before, the discrete states in the dot certainly will contribute to the bare charging energy according to Eq. (1). This is manifested in the aperiodic CB oscillations in Fig. 2(a). For dot 2 we find $\alpha \approx 0.154$ eV/V, $E_C \approx 41$ meV and $d \approx 30$ nm. Since the most pronounced conductance oscillations appear at a higher conductance than for dot 1, a higher occupation with electrons can be assumed, leading to a reduced influence of δE on the period of the conductance oscillations. Therefore a more metallic behavior can account for the more periodic conductance oscillations shown in Figs. 2(b) and 3(b). In order to investigate the properties of the confining potential at the $Si-SiO_2$ interface, we measured both the gate characteristic as well as the nonlinear source/drain characteristic as a function of magnetic field. In order to demonstrate the influence of a magnetic field on the energy levels of the dot, we evaluate a two-dimensional harmonic potential with eigenfrequency ω_0. In general, we expect the quantum mechanical level spacing to be strongly altered in a magnetic field if the confining potential is rather weak and if ω_0 is of the order of the cyclotron frequency ω_c. In Fig. 4(a) we show the magnetic field dependence of the gate characteristic of dot 1. In Fig. 4(b) the measurements of the nonlinear characteristic in various magnetic fields are presented. Obviously, in both measurements no significant influence of the magnetic field on the electrical properties can be observed and therefore the assumption of a hard-wall potential is justified. In Fig. 5(a) the temperature dependence of the gate characteristic is shown: clear CB oscillations up to temperatures above 100 K are visible. The first conductance maximum displays almost no change in shape in the temperature range between 2 and 100 K, whereas the subsequent oscillations at higher top gate voltages V_{TG} clearly begin to vanish towards higher temperatures. The etching process does not produce extremely steep steps in the SOI film and the profile of the quantum dot is therefore smaller at the top side of a SOI film than at the bottom. Strong inversion of the quantum dot naturally begins at the center of the structure proceeding to a complete inversion at higher V_{TG}. Therefore the effective capacitance of our device presumably is smaller at low V_{TG} than at high gate voltages. We examined the temperature dependence of

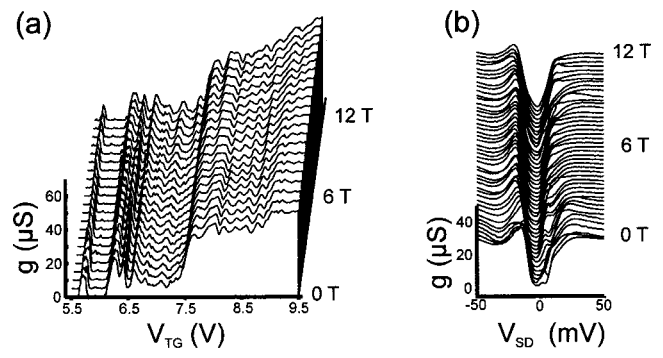

FIG. 4. (a) Magnetic field dependence of the Coulomb blockade oscillations and of the nonlinear $I_D - V_{SD}$ characteristic at $T=2$ K (b).

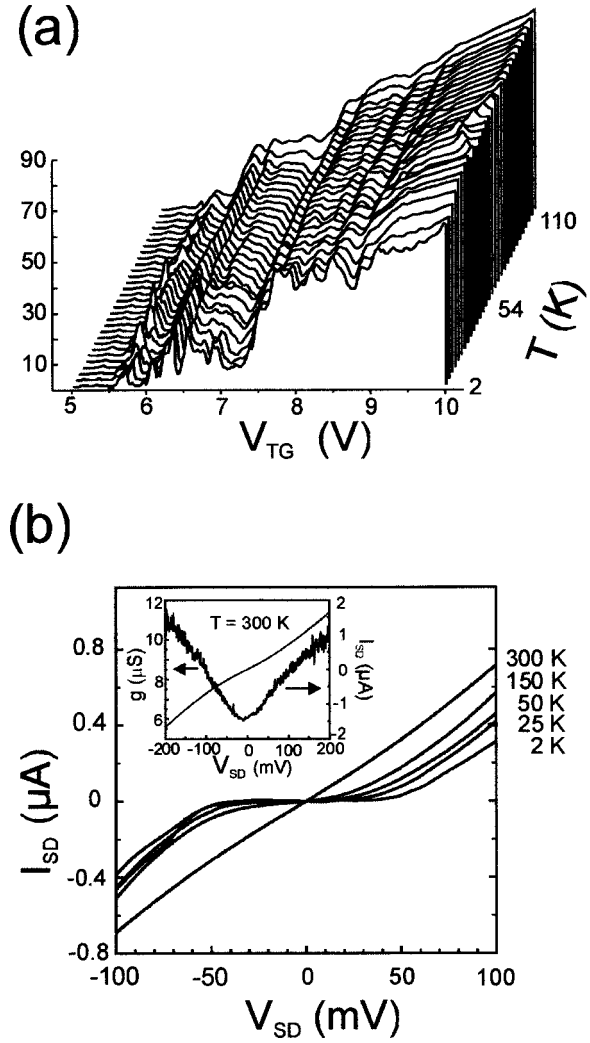

FIG. 5. (a) Temperature dependence of the conductance oscillations of dot 1. Note especially that the first conductance maximum is almost unaffected by the temperature rise up to 110 K. (b) Temperature dependence in the nonlinear bias regime. At $T=300$ K the Coulomb blockade gap remains visible.

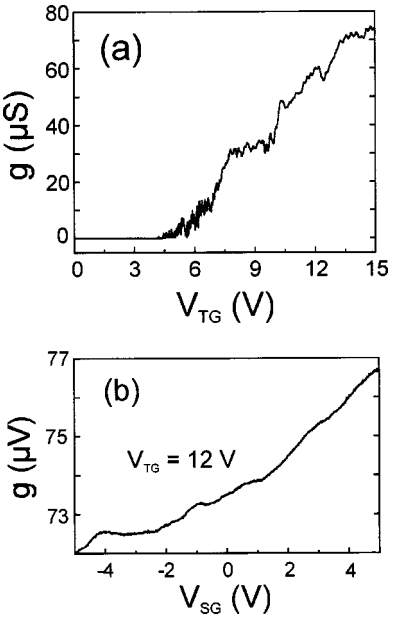

FIG. 6. (a) Gate characteristic of a 25-nm-wide and 500-nm-long wire. The features observed can be interpreted as electron interference effects, since no Coulomb blockade diamond could be found. (b) Conductance of a strongly inverted 25-nm-wide wire as a function of V_{SG} at fixed $V_{TG}=12$ V.

the nonlinear characteristic in more detail for the smaller dot [Figs. 2(a) and 3(a)], adjacent to the first conductance maximum [Fig. 5(b)]. A clear CB gap in the conductance is found even at room temperature. Since CB should remain visible up to temperatures of $T=E_C/2k_B\approx 310$ K in this device, this finding is in good agreement with the theoretical expectations.

B. Quantum wires

In contrast to the formation of electron islands by pattern-dependent oxidation,[8] width fluctuations in nanowires,[6] or in SOI quantum point contacts[7] we define the silicon nanostructures only by means of nanolithography. Therefore we are able to define the basic devices required for possible SET logic elements. In order to demonstrate the lithographic definition of the SET structures, we prepared SOI nanowires with various widths and lengths. In none of these nanowires CB oscillations could be observed. In Fig. 6(a) the conductance of such a 25-nm-wide nanowire is shown. Since we do not shrink our nanostructures by thermal oxidation as strongly as in Ref. 6, width fluctuations cannot lead to an accidental formation of electron islands. Therefore, our fabrication method is intended to be highly reproducible even at structure sizes in the 10 nm regime. Since we did not observe a Coulomb blockade diamond in this structure as judged by measuring the nonlinear I_D-V_{SD} characteristic the features observed in the gate characteristic of the nanowires cannot be attributed to CB oscillations similar to the ones seen in Fig. 2 under large top gate voltages ($V_{TG}>9$ V) where CB oscillations vanish. These features are similar to those observed by Leobandung *et al.*[5] in quantum dot structures. They are interpreted in terms of electron interference effects in the laterally structured 2DES enclosed on the nanometer scale. In high mobility 2DES in bulk silicon MOSFETs the phase coherence length L_Φ can be as large as 1 μm[11] at temperatures below 0.5 K. We therefore also believe that especially in narrow wires quantum interference might occur due to the geometry of the confined 2DES. In order to demonstrate functioning of the in-plane side gate, we measured the conductance of the 25-nm-wide wire as a function of side gate voltage V_{SG} at a fixed top gate voltage of $V_{TG}=12$ V which is large enough to drive both side gates and the wire into strong inversion. In Fig. 6(b) the conductance decrease for $V_{SG}<0$ V and the increase for $V_{SG}>0$ V demonstrate the feasibility of depleting the electron channel inside the nanowire. As an example of the application of these dual gate configurations for CMOS-based SET-logic circuits, we envision a SET inverter, one of the most important elements of a CMOS-based single-electron logic. Figure 7(a) shows the equivalent circuit for the inverter that mainly consists of two special SETs:[12] the so-called *p*-SET (in analogy to CMOS) conducts at gate voltages that lead to CB for the so-called *n*-SET and vice versa.

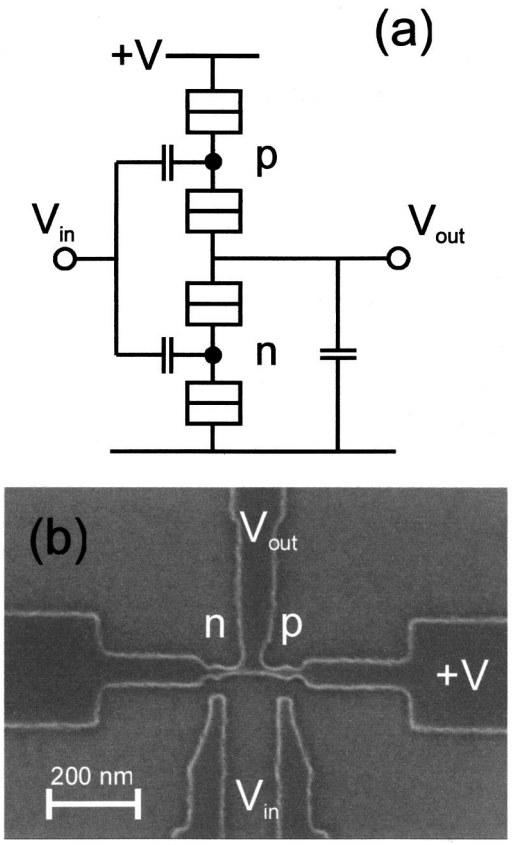

FIG. 7. (a) Equivalent circuit for a CMOS-based SET inverter according to Ref. 12. The so-called *n*-SET is in a conducting state at gate voltages that block the so-called *p*-SET and vice versa. (b) Realization of the SET inverted using in-plane side gates.

IV. CONCLUSION AND SUMMARY

In conclusion, we have demonstrated lithographic techniques to build a variety of silicon nanostructures. Coulomb blockade in quantum dots embedded into the 2DES of an SOI-MOSFET up to room temperature has been observed. The magnetic field dependence of the electrical parameters

demonstrates the robustness of the confining potential as well as the controllability of the source and drain tunnel junctions. We show that quantum wire structures fabricated by the same process do not display Coulomb blockade oscillations and therefore give evidence for the truly lithographic definition of our devices. By applying a voltage to an in-plane side gate, we can deplete and enhance the strongly inverted nanowire. This offers the possibility for individual tuning of quantum dots on the nanometer scale in an integrated SET logic as demonstrated for a SET-based CMOS circuit.

ACKNOWLEDGMENTS

The authors would like to thank L. Pescini and F. Simmel for stimulating discussions and A. Kriele, S. Manus, W. Kurpas, and P. Kiermeier for technical support. The authors acknowledge financial support from the German Ministry of Science (BMBF) Contract No. 01M2413C6 and the Deutsche Forschungsgemeinschaft in the Schwerpunkt Quanteninformationsverarbeitung (DFG-B1487/2-1).

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