Single-electron tunneling in highly doped silicon nanowires in a dual-gate configuration

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Lateral patterning of highly doped silicon-on-insulator films allows us to observe conductance oscillations due to single-electron charging effects. In our devices, silicon nanostructures are embedded into a metal–oxide–silicon configuration. The single-electron effects can be tuned both by an in-plane sidegate, as well as by a metallic topgate, a technology which is compatible with large-scale integration of single-electron devices with dimensions down to 10 nm. We compare the influence of different gating electrodes, important for ultralarge scale integration, on the electron islands. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1368399]

I. INTRODUCTION

Single-electron tunneling in silicon nanostructures has attracted considerable interest during the last few years. Due to the possible integration of these structures into standard complementary metal–oxide–silicon (CMOS) processes, these structures are believed to be promising candidates for future device applications. Using silicon-on-insolator (SOI) systems allows in addition a relatively simple fabrication of these structures by lateral patterning of SOI films. Up to now, several types of single-electron devices based on SOI have been realized,[1–5] leading to first single-electron transistors (SETs) operating up to room temperature.[2,6]

Smith *et al.*[3] fabricated conducting silicon nanowires with lateral dimensions down to about 50 nm using highly doped SOI material. They resolved conduction peaks by changing the voltage applied to an in-plane sidegate, also defined in the highly doped SOI film. Although the mean peak-to-peak spacing was constant in subsequent gate sweeps, both the exact peak positions as well as the peak amplitudes differed from run to run. This observation can be interpreted in terms of the formation of randomly distributed electron islands separated by tunneling barriers formed by dopant fluctuations inside the nanostructure. Since usually a serial arrangement of SETs is formed, no exact periodicity of the conduction peaks can be found in these structures. An enhancement of the Coulomb gap has been observed in the case, where the highly doped silicon nanostructure is almost depleted by the sidegate voltage.[7] This behavior is attributed to the formation of space-charge regions in series with the tunnel barriers formed by random dopant fluctuations.[8] Recently, single-electron effects in vertical SETs were also observed.[9]

In the present article we investigate highly doped silicon nanowires similar to those reported by Smith *et al.*[3] In addition to the common sidegate configuration in this work, we embedded both the highly doped nanowire as well as an in-plane sidegate in the gate oxide of a conventional MOS field effect transistor. This allows us to control the conductance oscillations of the nanowire by varying both the topgate voltage as well as the in-plane sidegate voltage.

II. FABRICATION OF HIGHLY DOPED SILICON NANOWIRES

We start fabrication of these silicon nanostructures by arsenic ion-implantation (dose $6.3\times10^{14}\,\mathrm{cm}^{-2}$, 20 keV) followed by rapid thermal annealing at 1000 °C for 30 s. In order to obtain thinner silicon films, a sacrificial thermal oxide is grown on the upper Si layer with a thickness of about 50 nm by rapid thermal oxidation (RTO), consuming 25 nm of silicon. After etching the oxide in buffered HF we define a mesa structure in the remaining 25 nm thick silicon film with alignment marks for the following electron-beam lithography step using conventional photolithography and reactive ion etching (RIE) in CF_4. Employing low-energy electron-beam lithography with the electron resist calixarene, we succeeded in defining nanowires with widths down to 9 nm, shown in Fig. 1.[10] The exposed resist is then used as an etch mask in an RIE process, which removes the unprotected silicon layer down to the buried oxide. Large contact regions are protected by a photoresist masking during the RIE process.

We subsequently grow a thin thermal gate oxide with a thickness of about 5 nm at 950 °C in order to passivate the etched structures and to anneal damages of the etching process near the structure's surfaces. A 50 nm thick oxide layer is then deposited either by chemical vapor deposition or by sputtering. Finally, a metallic topgate is provided by evaporation or sputtering.

The sample geometry is as follows: The in-plane sidegate is located at a distance of $a=95\,\mathrm{nm}$ from the nanowire with length $l=500\,\mathrm{nm}$ and width of about $w=10\,\mathrm{nm}$ and is embedded in the gate oxide. The metallic topgate is located above both the wire and the sidegate. The total gate oxide has a thickness of about $d=55\,\mathrm{nm}$. The silicon film thickness after thermal oxidation is estimated to be about h

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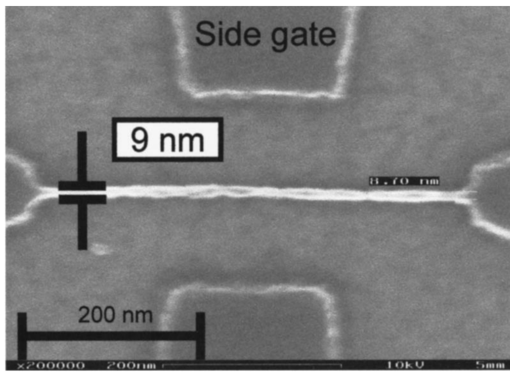

FIG. 1. Nanowire with a width of 9 nm defined in calixarene. This etch mask is transferred into the substrate. Shrinking of the silicon structure by thermal oxidation enables fabrication of silicon structures in the sub-10 nm regime.

$=25$ nm. A sketch of the cross section of the device is given in Fig. 2.

III. MEASUREMENTS

In Fig. 3 we show the conductance of the wire defined as $g=dI_D/dV_{\mathrm{SD}}$ as a function of topgate voltage V_{TG} at a temperature of 2 K with I_D the drain current and V_{SD} the source–drain voltage: Almost periodic conductance peaks are observed. Similar to the observations reported by Smith and Ahmed[3] the absolute position of these peaks as well as their amplitude are not stable in time. It was therefore not possible to resolve a clear Coulomb blockade diamond required to derive the conversion factor α defined by

$$\alpha=eC_G/C \tag{1}$$

with the gate capacitance C_G for an arbitrary gate electrode and the total capacitance C of an electron island assumed to have formed spontaneously in the nanowire. The conversion factor α is required to evaluate the gate capacitance, since it relates to the Coulomb charging energy E_C defined by

$$E_C=\alpha\Delta V_G, \tag{2}$$

with ΔV_G being the period of the conductance oscillations as a function of topgate V_{TG} or sidegate V_{SG} voltage, respectively. In order to derive the Coulomb charging energy of the

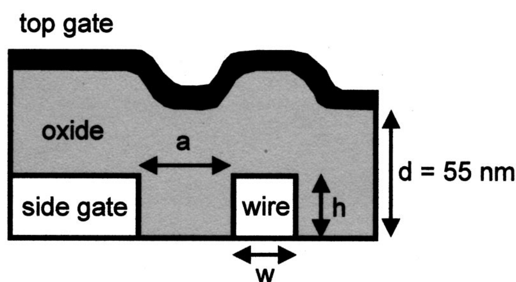

FIG. 2. Sketch of the device: The in-plane sidegate is located at a distance $a=95$ nm from the silicon nanowire with a width $w=10$ nm and a length of $l=500$ nm. The silicon film thickness is estimated to be about $h=25$ nm. Both structures are embedded into SiO_2, acting as gate oxide with a thickness of $d=55$ nm. On top, a NiCr/Au gate is located, controlling the electric potential in both the nanowire and the sidegate.

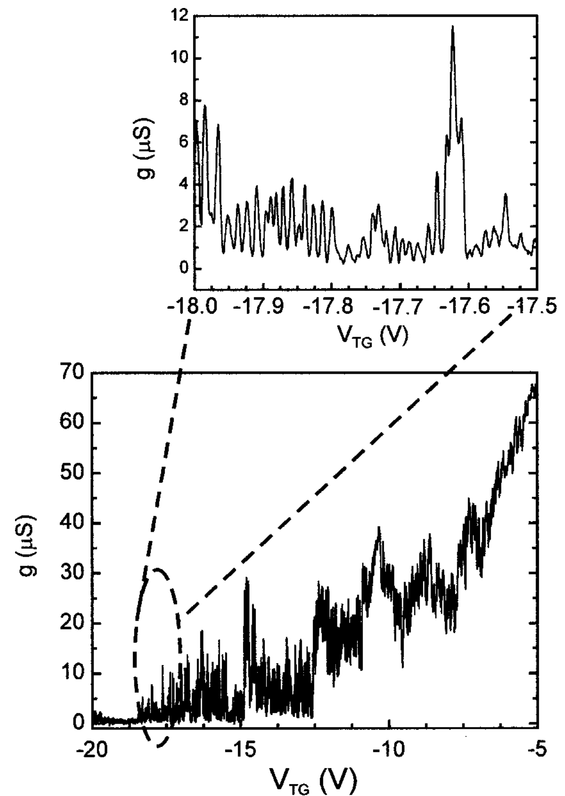

FIG. 3. Single-electron effects in a highly doped, 10 nm wide silicon wire at $T=2$ K as a function of the topgate voltage V_{TG}. Although almost periodic conductance oscillations can be found, both the peak amplitudes as well as the exact peak positions differ between subsequent gate sweeps.

spontaneously formed electron island as a function of gate voltage, we used a conversion factor $\alpha\approx 50$ meV/V, observed in similar structures.[5]

Using this value and assuming the conduction peaks to be Coulomb-blockade (CB) oscillations in randomly formed metallic islands inside the wire, we derive a charging energy of $E_C\approx 0.7$ meV. This value clearly is too small to result from only one electron island with a lateral dimension of $\sim$20 nm. Also the temperature dependence of the nonlinear source–drain characteristics shown in Fig. 4, as well as of the gate characteristics (not shown here) clearly contradict a charging energy below 1 meV. Since CB should vanish when the thermal energy exceeds about half of the charging energy, no effect of single-electron charging is expected to remain visible above 4 K. We therefore interpret our results in terms of the formation of multiple tunnel junctions (MTJ) similar to Ref. 3. Here, regions with low conductivity are formed by random dopant fluctuations. Assuming statistic dopant fluctuations to be proportional to $\sqrt{N_D}$ with the donor concentration N_D,[11] these fluctuations should only be around 10^{10} donors per cm^3. Since both common n dopants for silicon, As and P pile up during dry oxidation with a segregation coefficient of about 10,[12] the dopant fluctuations due to segregation effects should be dominant in the process of MTJ formation. Since the geometry of nanoscale structures is very important for the oxidation rate,[13] edge roughness presumably can lead to a strong modulation of dopant concentration along the oxidized silicon nanowire. In terms of

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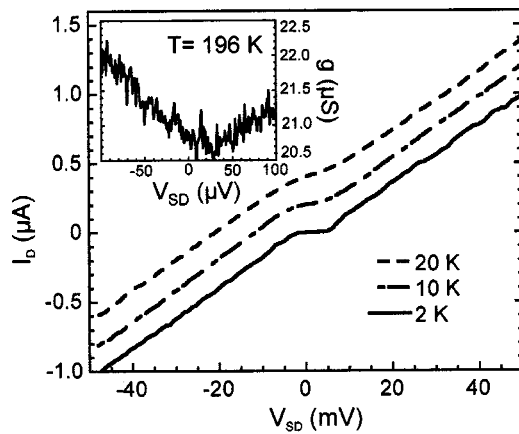

FIG. 4. Temperature dependence of the I_D-V_{SD} trace. The wire shows a distinct nonohmic behavior at temperatures up to 20 K. Single-electron effects remain visible only weakly up to temperatures of about 200 K (see inset).

MTJ no charging energy E_C can be defined since electron tunneling occurs as a series of sequential tunneling events through a serial arrangement of tunnel junctions. Nevertheless, the good periodicity found in these structures still remains a striking result.

By setting the topgate voltage to a value near pinch-off, one can also observe conductance oscillations in our devices by changing the sidegate voltage V_{SG} (Fig. 5). This allows one to minimize the controlling sidegate voltage that is of special importance for possible applications of these devices in integrated circuits. Since the conversion factor α is not equal for the topgate and the sidegate, the mean period of the conductance oscillations changes when controlled by the different gates. Additionally, the oscillations as a function of the sidegate voltage V_{SG} seem to be not as periodic as controlled by V_{TG}. In Fig. 6 we compare the distribution of the peak spacings ΔV_{TG} and ΔV_{SG} from the measurements shown in Fig. 3 and Fig. 5. In Fig. 6(a) the distribution for ΔV_{TG} is shown and in Fig. 6(b) the distribution for ΔV_{SG} is shown. It is clearly visible that the distribution of the peak spacing is broader when the oscillations are controlled via the sidegate. The standard deviation for the distribution in Fig. 6(b) $\sigma_{SG}=0.43$ is larger than $\sigma_{TG}=0.32$ in Fig. 6(a).

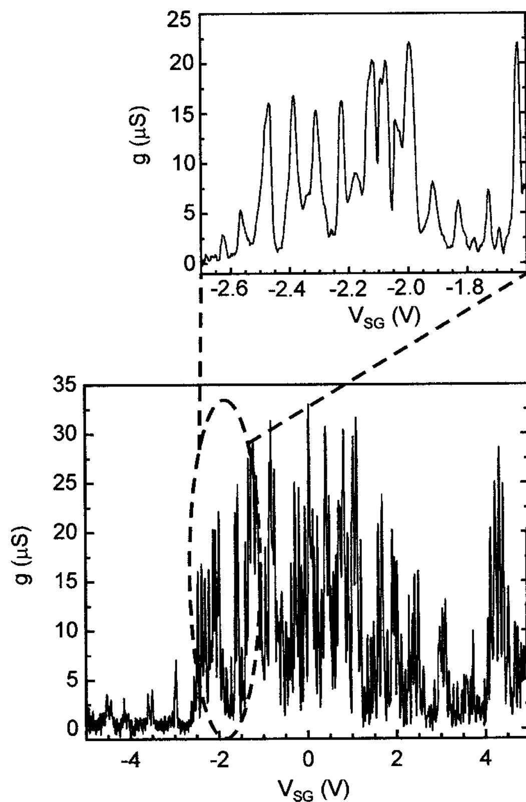

FIG. 5. By controlling the electrostatic potential of the wire via an in-plane sidegate conductance oscillations can also be observed. The mean period of these oscillations differs from that observed in Fig. 3. The topgate voltage in this measurement is $V_{TG}=17.5$ V, which allows low sidegate voltages to control the CB oscillations.

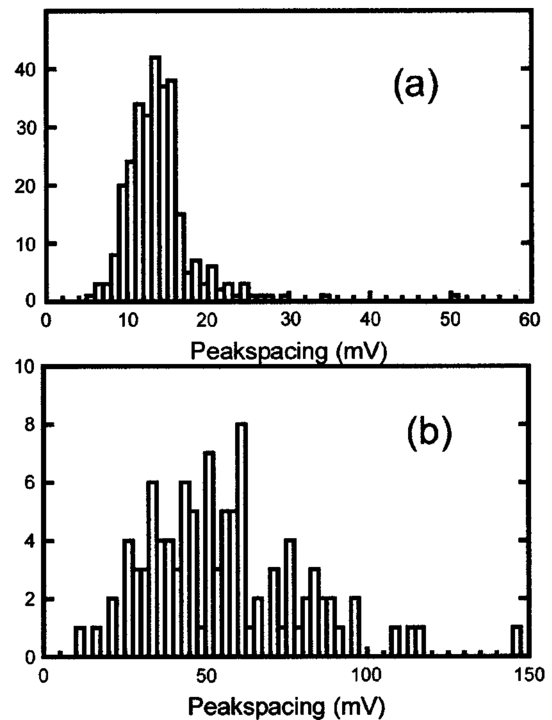

FIG. 6. Distribution for the peak-to-peak spacings found in Figs. 3 and 5. The histogram in Fig. 6(a) shows the distribution for V_{TG}, in Fig. 6(b) the curve for V_{SG} is shown. The curve in Fig. 6(b) clearly shows a larger broadening than the plot in Fig. 6(a). The standard deviation for the distribution in Fig. 6(a) is $\sigma_{TG}=0.32$ and in Fig. 6(b) $\sigma_{SG}=0.43$.

Formation of MTJs inside the silicon nanowire by applying a negative topgate voltage also depletes the silicon sidegate. Since the dimensions of the sidegate are of the order of 100 nm it is reasonable to assume the formation of strong potential fluctuations also inside this highly doped silicon structure. These potential fluctuations are modulated by changing V_{SG} since the voltage between the sidegate and topgate is then also varied. This change in the potential landscape of the side-electrode by sweeping V_{SG} can therefore be made responsible for a stronger variation of the peak–peak spacing for the conductance peaks as a function of V_{SG} in comparison to that controlled by V_{TG}.

Since the operating point of common CB devices as well as of conventional MTJ structures has to be controlled via one gate voltage and is usually not reproducible for different

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devices,[14] the possibility to control the electric properties of these structures via two independent electrodes is of great importance. In our approach, the fabrication of larger single-electron circuits becomes feasible by setting each individual silicon nanowire to its operating point via either V_{SG} or V_{TG} and controlling the switching state of the wire by changing the other gate voltage.

In order to achieve a better understanding of these dual gate structures, we compare the capacitances between randomly formed electron islands within the silicon nanowire and the topgate and sidegate, respectively. The ratio between these capacitances can be easily determined by comparing the mean peak-to-peak spacing in Figs. 3 and 5. The total capacitance C of such an island can be written both in terms of C_{TG} and of C_{SG} using the conversion factors α defined in Eq. (1)

$$C=\frac{e}{\alpha_{TG}}\cdot C_{TG}=\frac{e}{\alpha_{SG}}\cdot C_{SG}. \tag{3}$$

The ratio of C_{TG} and C_{SG} can be easily calculated to $C_{SG}/C_{TG}=\Delta V_{TG}/\Delta V_{SG}\approx 0.25$. For the simulation of the topgate and sidegate capacitance, respectively, we used an electromagnetic finite element program (MAFIA[15]). Approximating C_{TG} by the capacitance of a conductive sphere with a distance of 55 nm to a conductive plane leads to $C_{TG}\approx 2.0$ aF.

In analogy, the sidegate capacitance of a 25 nm high, 200 nm wide, and 95 nm separated electrode with respect to a conductive sphere (10 nm in diameter) is estimated to be about 0.38 aF. The theoretically estimated value for the ratio of the two capacitances gives therefore $C_{SG}/C_{TG}\approx 0.19$, which is of the same order as the measured value.

IV. SUMMARY

In summary, we have observed conductance oscillations due to single-electron effects in a highly doped silicon nanowire that can be controlled via a metallic topgate as well as by an in-plane sidegate also realized in the doped SOI film. The distribution of the conduction peaks as a function of V_{SG} displays a larger standard deviation than that controlled by V_{TG}. This can be interpreted in terms of random potential fluctuations inside the side electrode changed by both V_{SG} and V_{TG}. Since single-electron devices commonly suffer from the poor reproducibility of the operating point, the possibility to control their electrical properties via two gates is of special importance for future applications. Furthermore, setting the topgate voltage to a value near pinch-off allows one to minimize the controlling sidegate voltage that is of special importance for possible applications of these devices in low-power integrated logic circuits.

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