Coulomb blockade in quasimetallic silicon-on-insulator nanowires

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Using highly doped silicon-on-insulator (SOI) films, we demonstrate metallic Coulomb blockade in silicon nanowires at temperatures up to almost 100 K. We propose a process that leads to island formation inside the wire due to a combination of structural roughness and segregation effects during thermal oxidation. Hence, no narrowing of the SOI wire is necessary to form tunneling contacts to the single-electron transistors. © *1999 American Institute of Physics.* [S0003-6951(99)03549-4]

Single-electron transistors (SETs) in silicon-based semiconductor nanostructures offer the interesting possibility to combine well-established silicon technology with the physical concepts of SETs. In contrast to quantum-dot devices in high-mobility GaAs/AlGaAs heterostructures, where the depletion length of the two-dimensional electron system limits its lateral dot sizes to about 100 nm, the use of silicon-on-insulator (SOI) structures with ultrathin silicon films leads to structure sizes down to a few 10 nm. Since the capacitance between the quantum dot and the controlling gate structure determines the temperature range in which the SET reliably operates, the miniaturization of SET devices is the most demanding goal for future device applications at room temperature.

To date, two different approaches to realize ultrasmall SOI SETs have been implemented: Leobandung *et al.*[1] and others[2,3] used an inversion field-effect structure combined with lateral patterning of the SOI film and a source/drain implantation. Although Coulomb blockade is observed, a strong contribution of the large quantum-mechanical energy spacing levels crucially offsets the classically expected periodicity of the conductance peaks. According to the canonical theory of Coulomb blockade for SETs, the large number of electrons inhibits the separation of discrete energy levels, and the charging energy for adding one electron to the SET is ideally not perturbed by the single-particle energy states.

The second approach focuses on the use of highly doped SOI films and lateral structuring to obtain SOI wires.[4,5] In these devices, quantum-dot-like structures are naturally formed by the randomly occurring fluctuations of the dopant concentration. Usually, these lead to some serial SET structure and, consequently, these devices mostly lack a clear periodicity of the observed conduction peaks.

In our approach, the use of well-established SOI technology is combined with the fabrication of quasimetallic SETs by extremely high doping of the SOI films. This is of fundamental importance since metallic SETs offer many similar charging states and, hence, a broad range of operating points. Whereas earlier doping levels of about $10^{19}\,\mathrm{cm}^{-3}$ were common, leading to a mean distance between two dopant atoms of 4.6 nm, our samples have a nominal doping level of $10^{21}\,\mathrm{cm}^{-3}$. This leads to a mean distance of only 1 nm. Therefore, the distribution of dopant atoms can be assumed to be much more isotropic for an unprocessed wafer. The electron number in an ideal dot fabricated from this material with dimensions of about 50 nm is estimated to be about 10^5.

The unprocessed SOI wafers had a silicon film thickness of 50 nm with As ion implanted (dose $2\times10^{15}\,\mathrm{cm}^{-2}$ at 10 keV) and a buried oxide thickness of 400 nm. The doping level was determined by Hall measurements to be about $5\times10^{20}\,\mathrm{cm}^{-3}$, suggesting that not all dopants were activated during the annealing process in a rapid thermal annealing (RTA) chamber.[6] In order to obtain thinner silicon films, a thermal oxide was grown in the RTA chamber on the SOI wafers with a thickness of about 44 nm, consuming 20 nm of silicon. In the remaining 30-nm-thick, highly doped silicon film we defined a mesa structure with alignment marks for the following electron-beam lithography step using conventional photolithography and dry etching with CF_4. Using high-resolution low-energy electron-beam lithography and the negative electron resist calixarene,[7] we succeeded in preparing silicon wires with a lateral extension of about 15 nm by reactive-ion-beam etching with CF_4. The etched silicon structure is passivated by the growth of a low-temperature (950 °C, 16 min) silicon oxide of about 15 nm thickness followed by depositing 70 nm SiO_2 on top of the sample by passive or active sputtering. Finally, a metallic top gate and bond pads are evaporated. Figure 1 shows a schematic drawing of our device and in Fig. 2 a scanning electron-beam microscope (SEM) picture of an etched, but not yet oxidized, quantum wire is shown.

The temperature-dependent conductance of these silicon wires was measured in a ^{4}He bath cryostat with a variable temperature insert, allowing continuous operation from 1.5 to 200 K. Figure 3(a) depicts the conductance of a 50-nm-wide nanowire at a temperature of 4.2 K as a function of applied gate voltage. Oscillations with a clear periodicity are observed, indicating the metallic nature of the SET. On the other hand, the high offset in the valleys of the conductivity indicates parallel conductance, as will be discussed later. In

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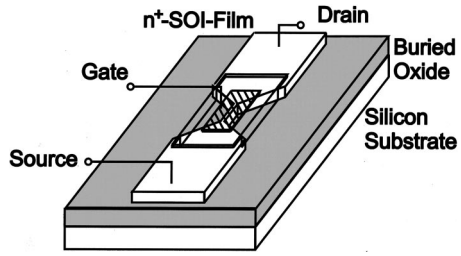

FIG. 1. Silicon-wire single-electron transistor in a highly doped SOI film. After passivation of the etched structure by growing a thin thermal oxide, a 70-nm-thick SiO_2 gate oxide and a metallic gate are deposited on top of the structure.

Fig. 3(b) we display a contour plot of the channel differential conductance versus top-gate voltage V_G and source/drain bias V_{SD}. From the slope of the Coulomb-blockade diamonds, which are only weakly pronounced due to the parallel conducting path, we determine the energy-level separation in the dot using the conversion factor

$$\alpha = \delta\mu(N)/\delta V_G = \tfrac{1}{2} e dV_{G,\diamond}/dV_{SD}, \tag{1}$$

with the chemical potential $\mu(N)$ of the dot charged with N electrons and $V_{G,\diamond}$ the edge of the diamond in Fig. 3(b). We obtain a value of $\alpha = 0.033\,\mathrm{eV/V}$ and a charging energy $E_C = 17.5\,\mathrm{meV}$. This leads to a total capacitance of $C_\Sigma = 10^{-17}\,\mathrm{F}$. With the straight-forward estimation of a cylindrically shaped island with the axis perpendicular to the surface, we calculate the island diameter to be about 70 nm. Presumably, the real island formed has a larger extension along the wire than perpendicular to it. Therefore, this value is in good agreement with the dimensions found in the SEM micrographs.

In Fig. 4 the temperature dependence is presented: The oscillations remain visible up to a temperature above 70 K. Since the Coulomb blockade should not be affected unless the thermal energy kT exceeds half of the charging energy $E_C = e^2/C_\Sigma$, this result suggests a charging energy of about 15 meV. Furthermore, fitting the shape of the conductance peaks with a full width at half maximum $\Delta V_{1/2}$ in Fig. 4, we can also find a value for α and, therefore, for the charging energy[8] of the quantum-dot structure according to

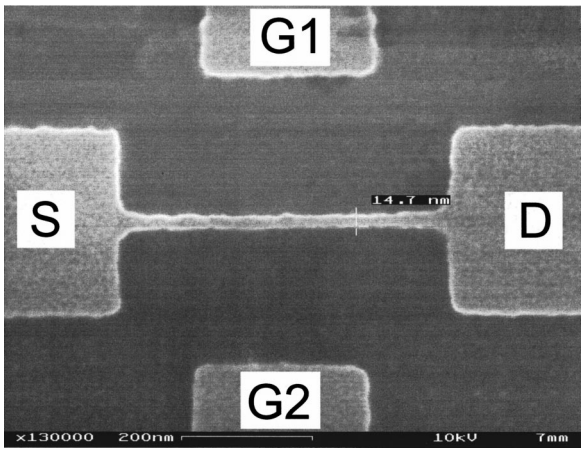

FIG. 2. Scanning electron-beam micrograph of an etched, but not yet oxidized, and gated silicon wire. The lateral dimensions can be scaled down to about 15 nm.

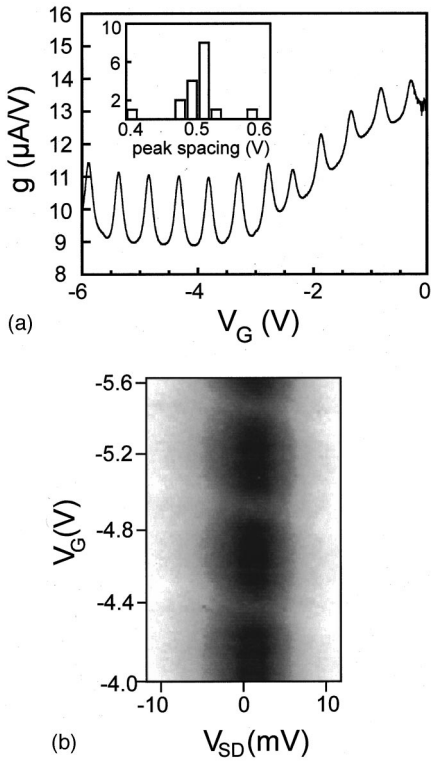

FIG. 3. (a) Coulomb-blockade oscillations in a highly doped 50-nm-wide silicon nanowire at 4 K. The peaks are almost perfectly equidistant. The inset shows the distribution of the peak spacing, being very close to 0.5 V. (b) Coulomb-blockade diamond: the slope of the diamond allows the calculation of the level charging energy.

$$\alpha = \frac{5 k_B \Delta T}{e \Delta V_{1/2}} \operatorname{arcosh}\sqrt{2}. \tag{2}$$

We obtain $\alpha \sim 0.12$ and a charging energy $E_C = 63\,\mathrm{meV}$, which differs strongly from the value calculated using the Coulomb-blockade diamond. We believe that the shape of the peaks is influenced by the apparent conductivity of the parallel channel in the nanowire leading to this deviation.

Generally, the formation of SETs inside doped silicon-wire structures is attributed to random fluctuations of the doping level inside the silicon film, causing lateral electric-field variations.[5] However, as the doping level is extremely high, it is not reasonable to assume that this effect causes the deviation in our device. Presumably, the pattern-dependent two-dimensional oxidation of laterally structured SOI de-

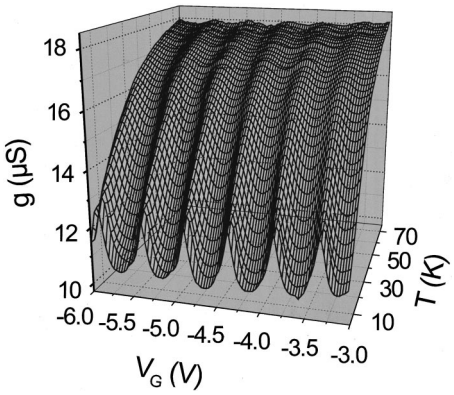

FIG. 4. Temperature dependence of the conductance peaks—the oscillations remain visible up to more than 70 K.

vices in combination with the pileup effect of As dopants during dry oxidation and edge roughness of the etched wire lead to the observed SET structure. Since the thermal oxidation of nanometer-scale curved structures is extremely sensitive to the geometry, in particular, to the radius of curvature, the oxidation rate can vary significantly along a Si wire with some edge roughness.[9] Since As piles up in silicon during dry oxidation due to a segregation coefficient of about 10,[10] this effect presumably also leads to a very inhomogeneous dopant concentration along the wire. Also, the formation of SiAs precipitates has been observed recently under similar conditions.[11] Our observation of a relatively high parallel conductivity can also be explained in this picture, suggesting the formation of a SET at one edge of the wire, where at the other edge a wire with Ohmic conductance still remains.

In conclusion, we here demonstrated the fabrication of a SET device in a highly doped silicon nanowire. We find equidistant conduction peaks in the gate characteristics, a typical indication for a metallic SET. We believe that this effect is caused by the segregation of dopants during the thermal oxidation in combination with the structural roughness. Nevertheless, effects of unintentional nonuniform dopant distribution presumably caused by spontaneous segregation cannot be ruled out. The metallic properties and the small capacitance of these devices place them in the range of interest for device applications.

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